

FIG. 1A

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and
Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

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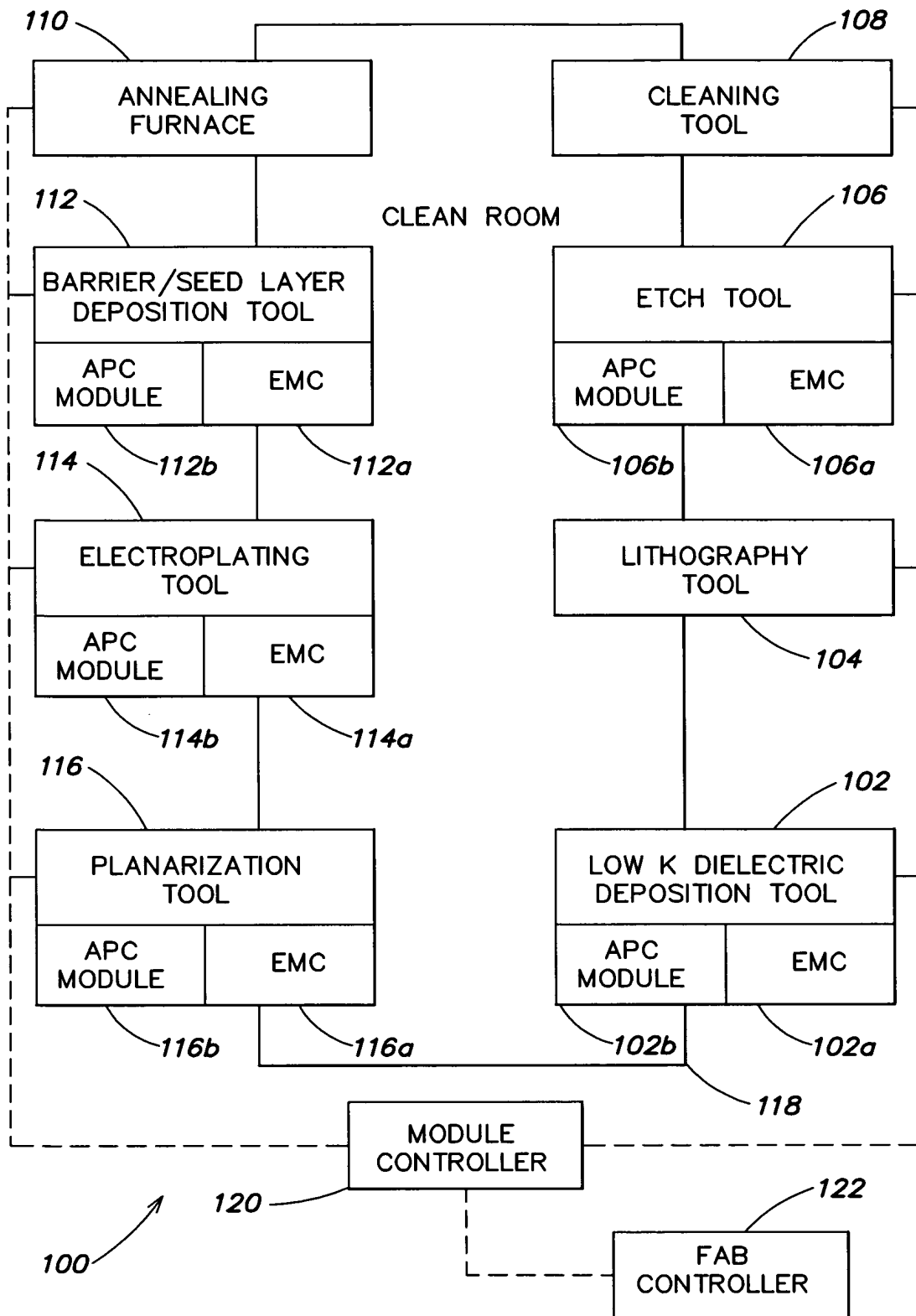


FIG. 1B

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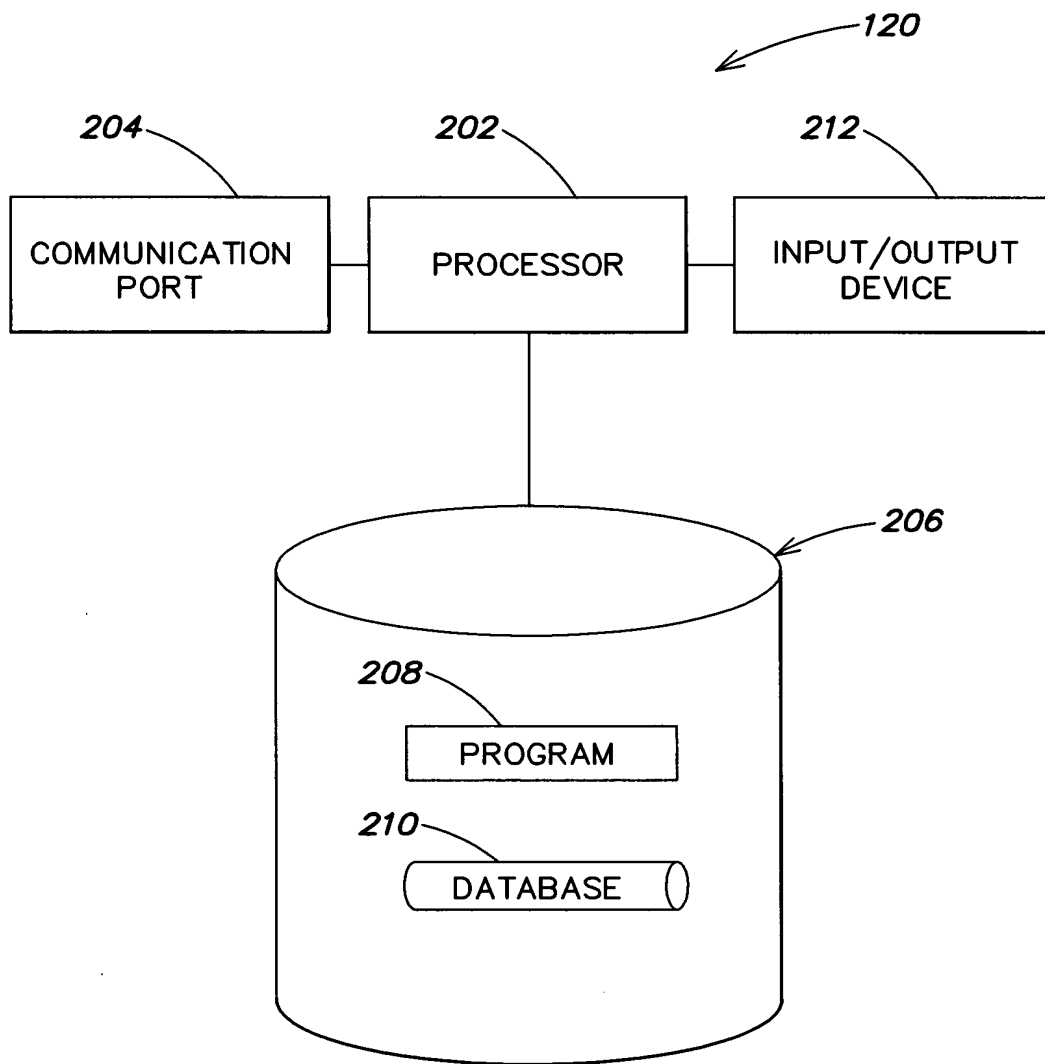


FIG. 2

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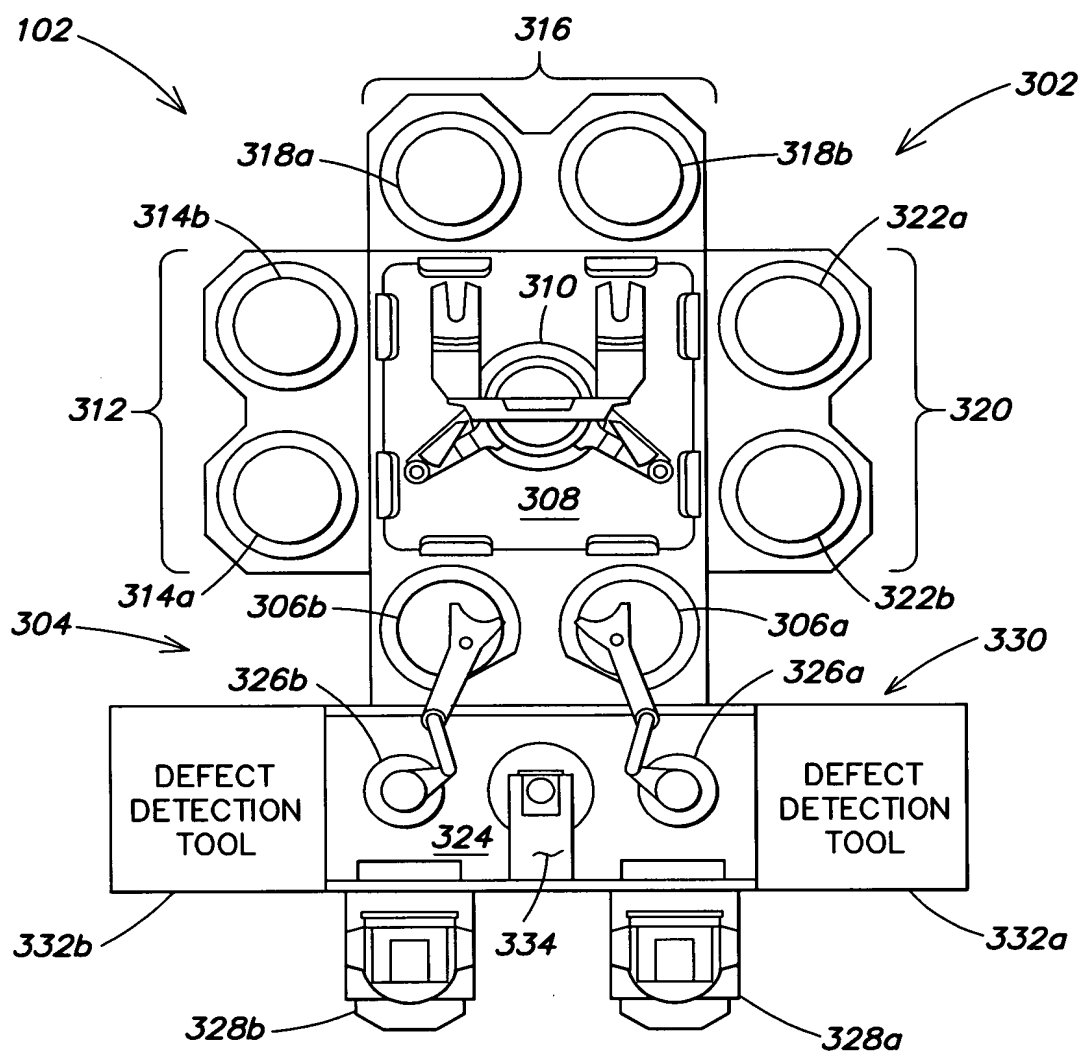
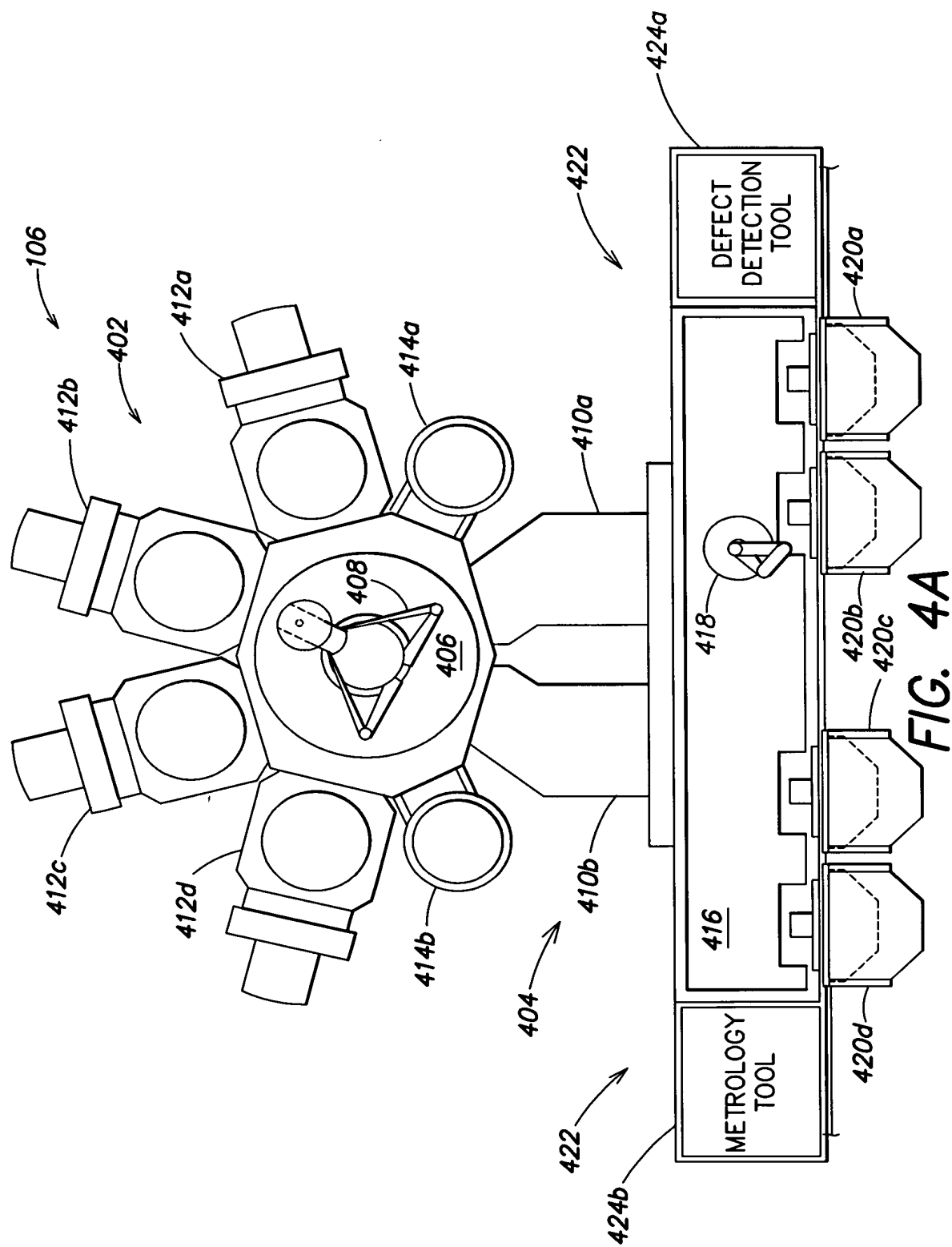


FIG. 3

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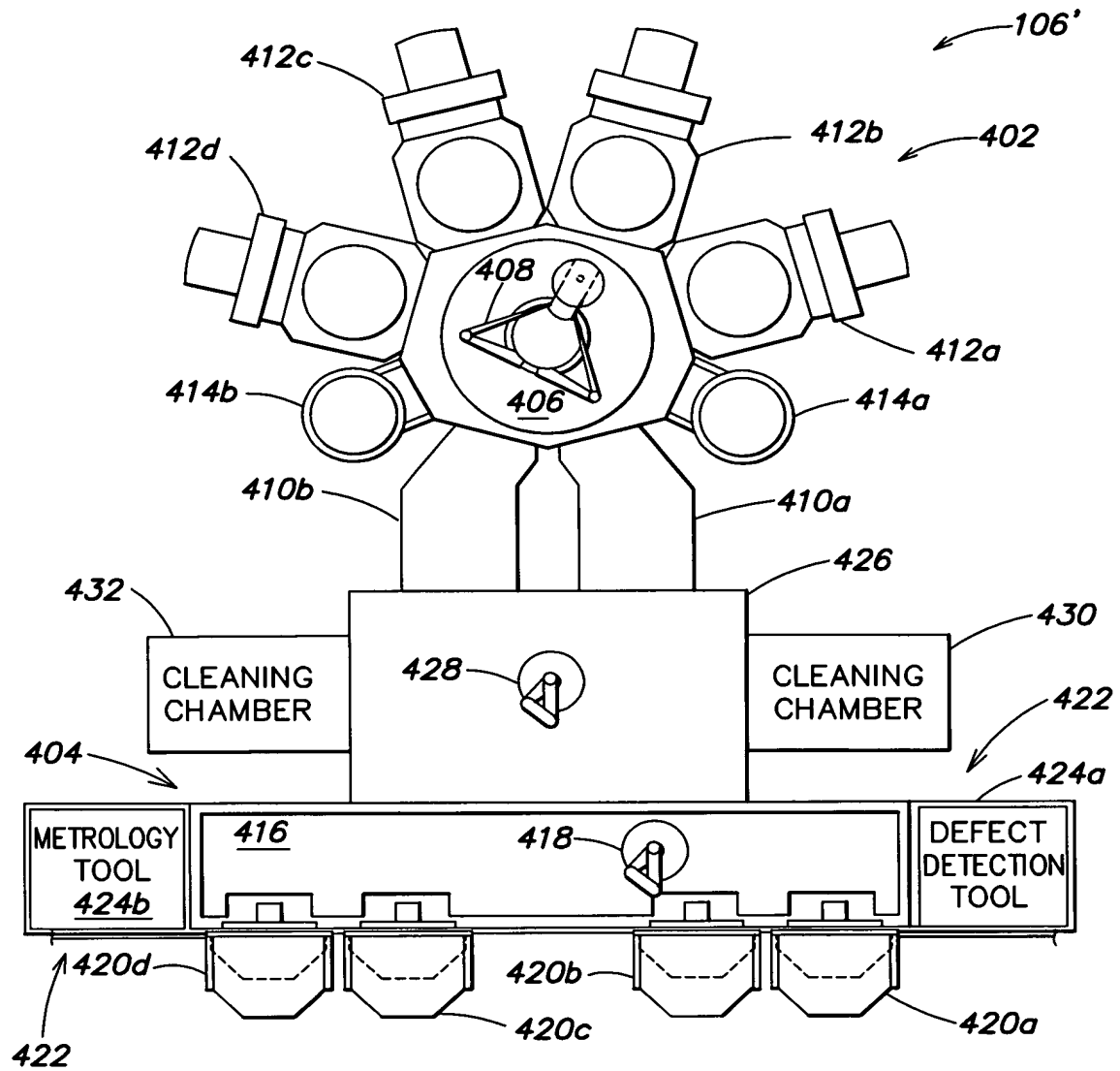


FIG. 4B

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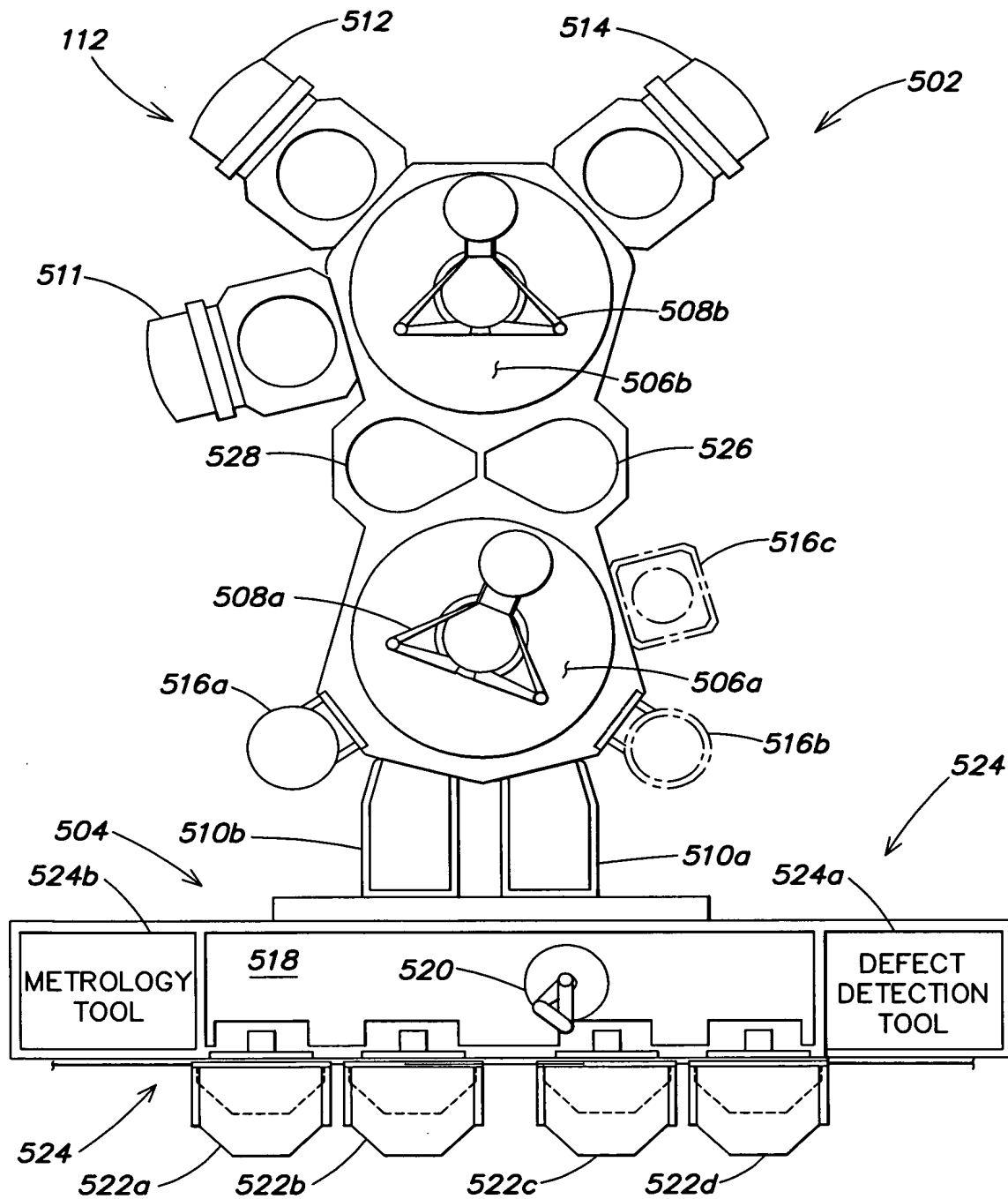


FIG. 5

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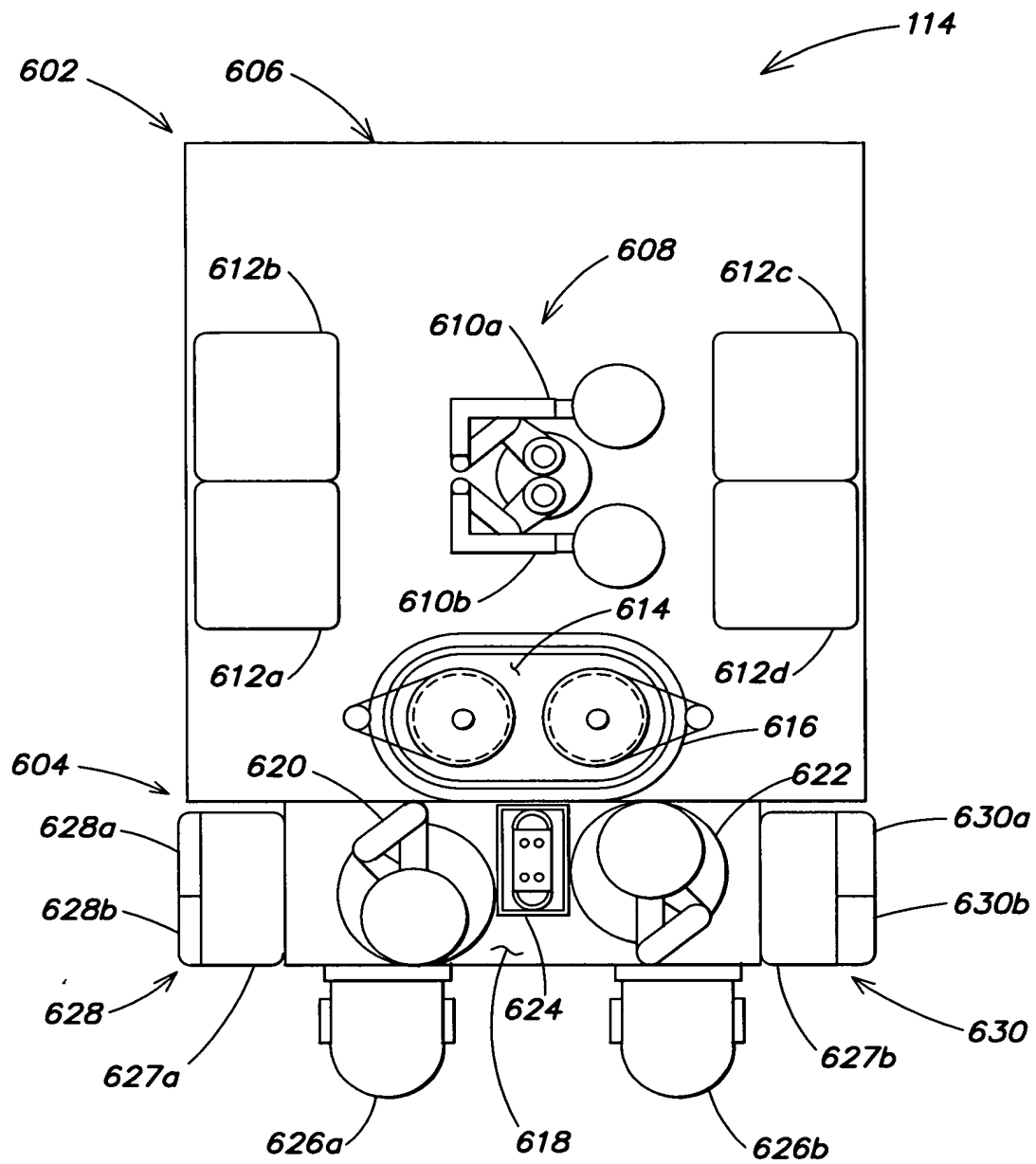


FIG. 6

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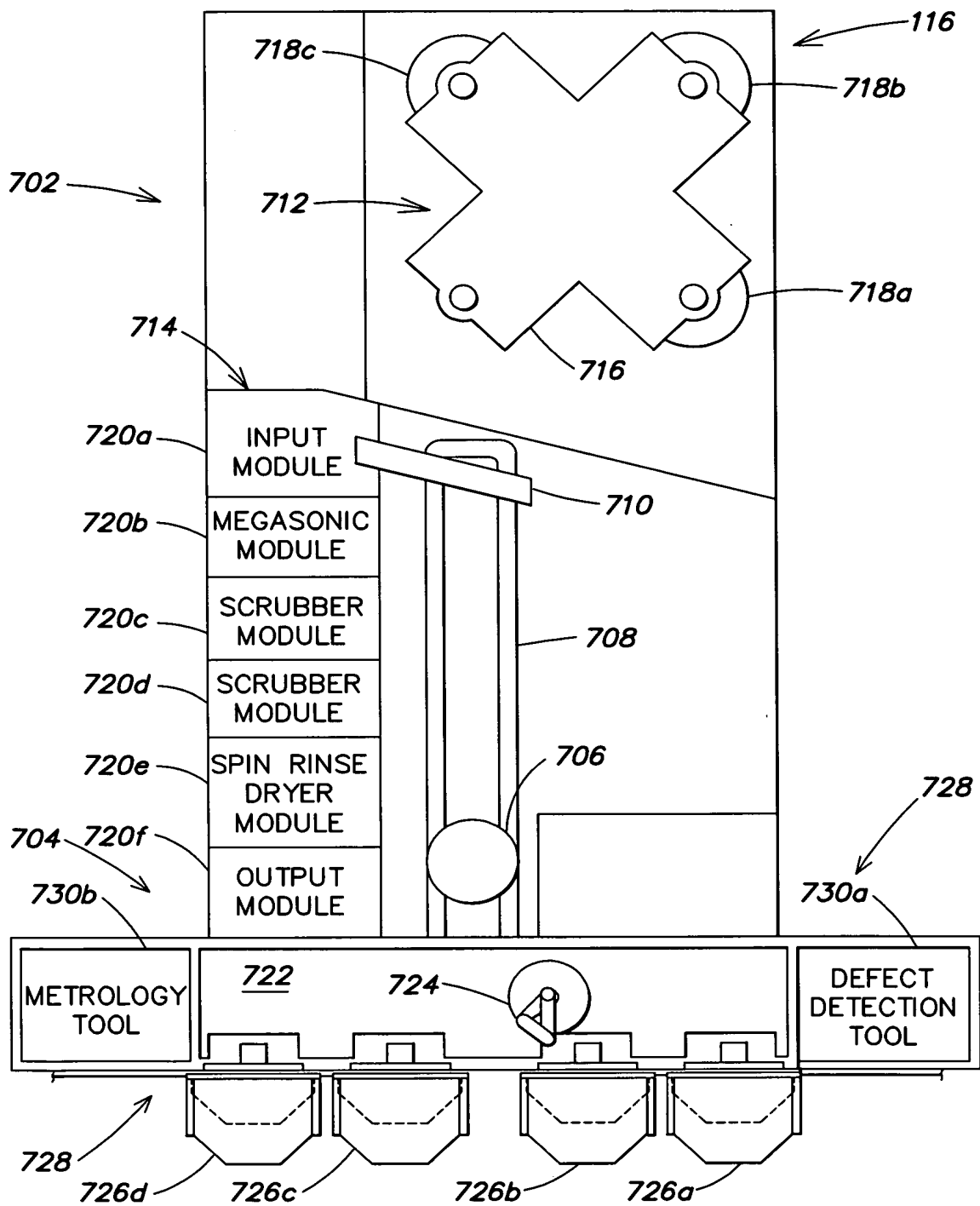


FIG. 7A

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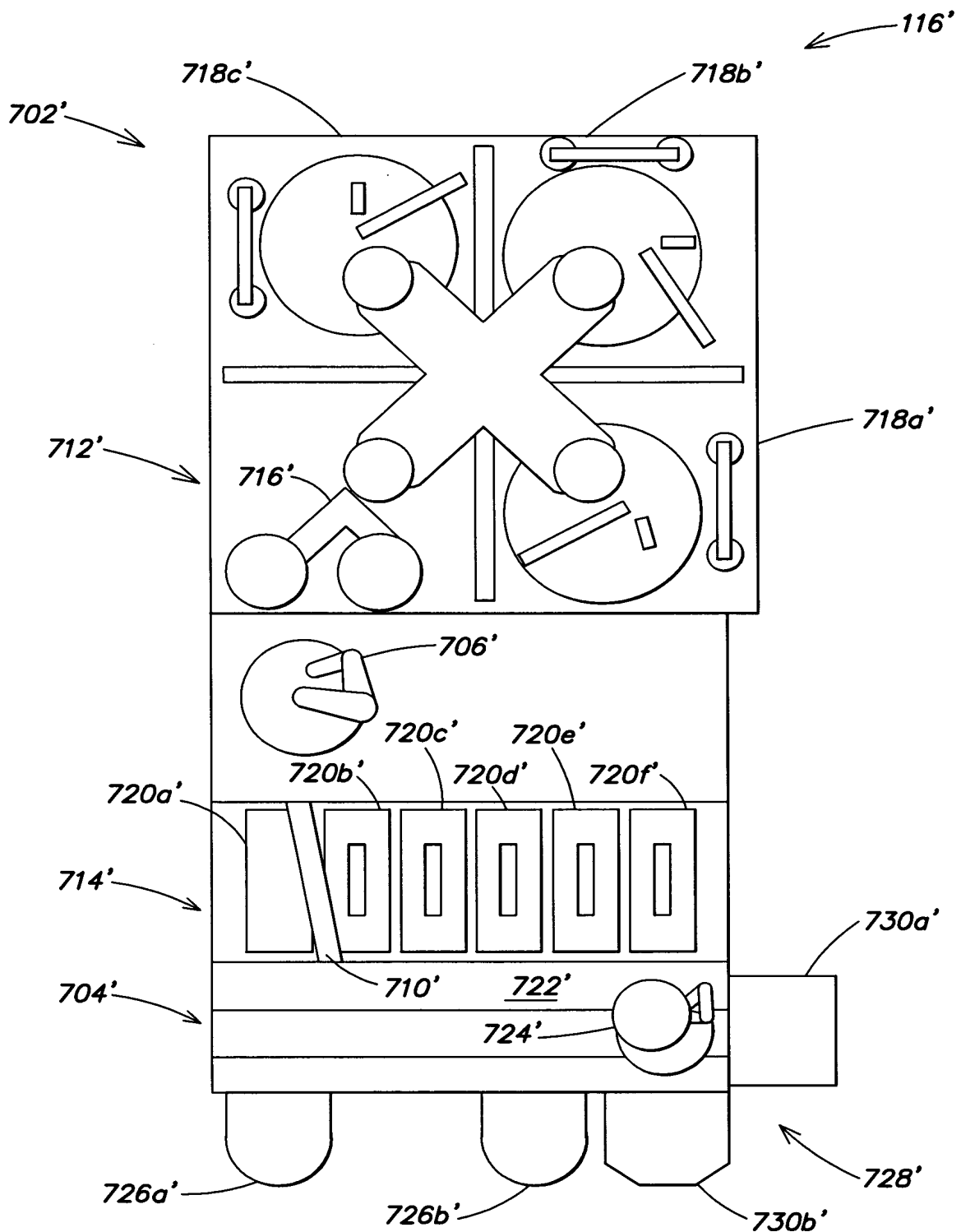


FIG. 7B

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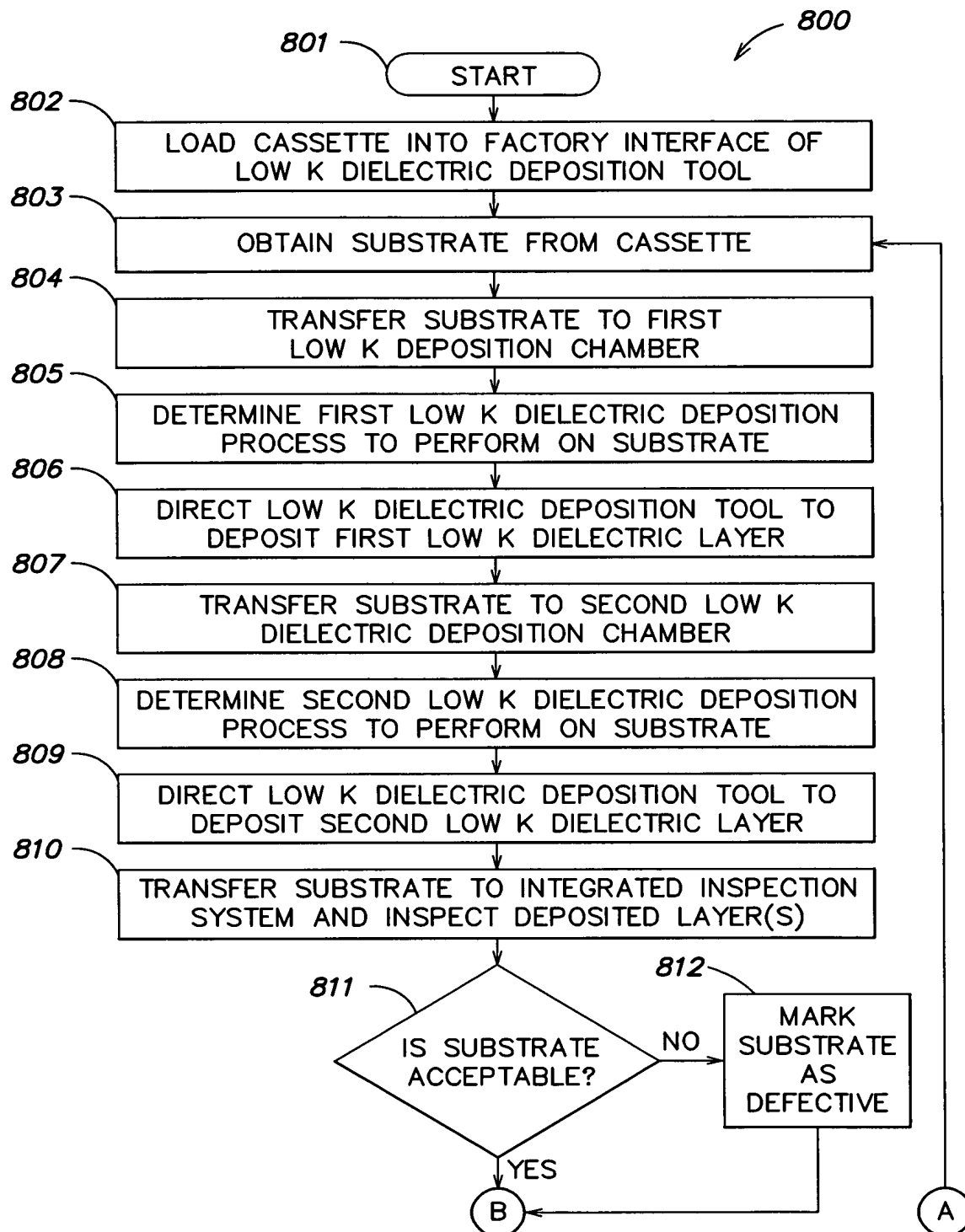


FIG. 8A

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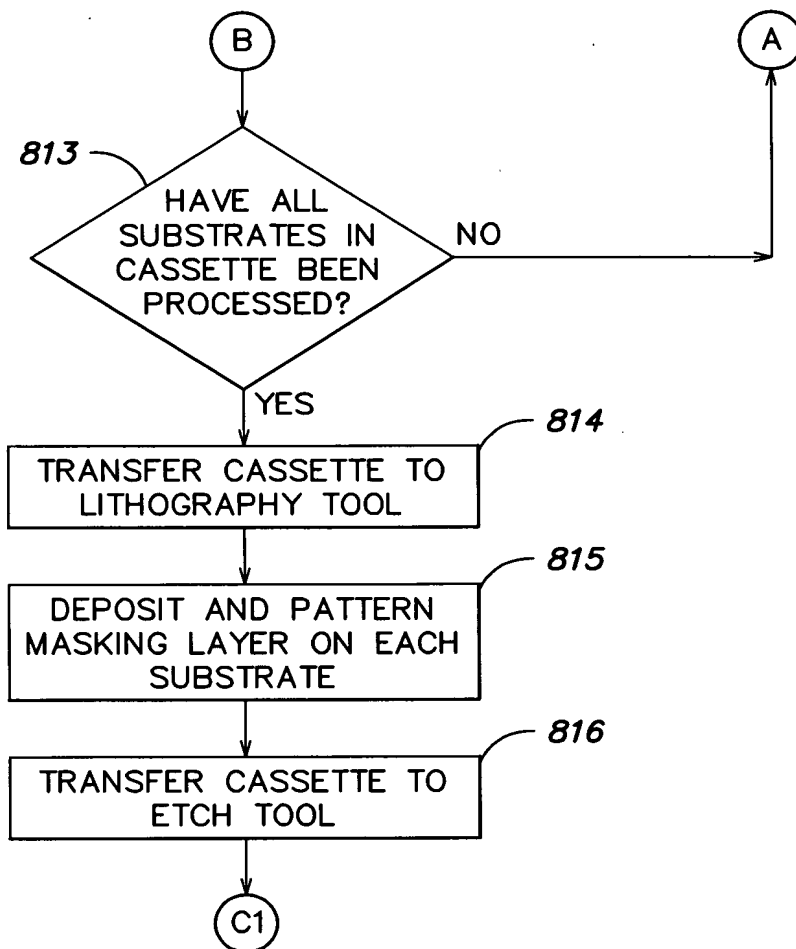


FIG. 8B

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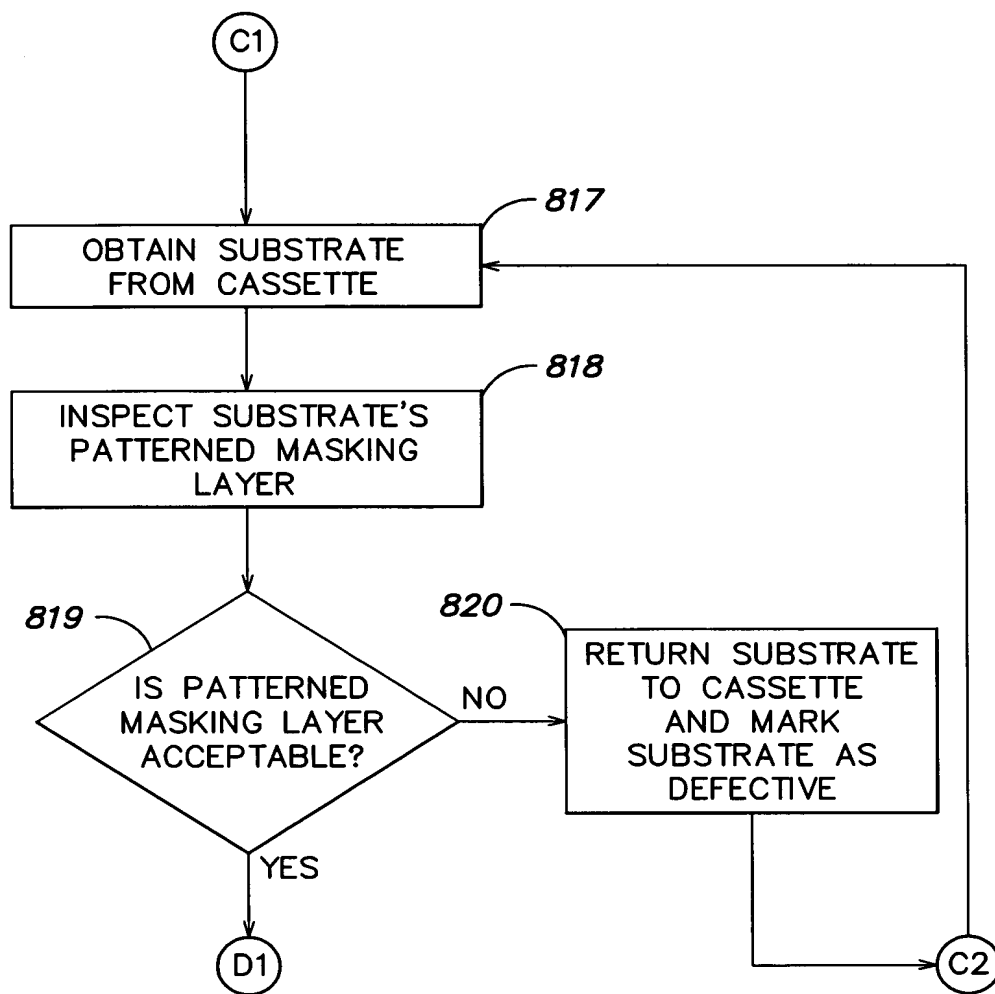


FIG. 8C

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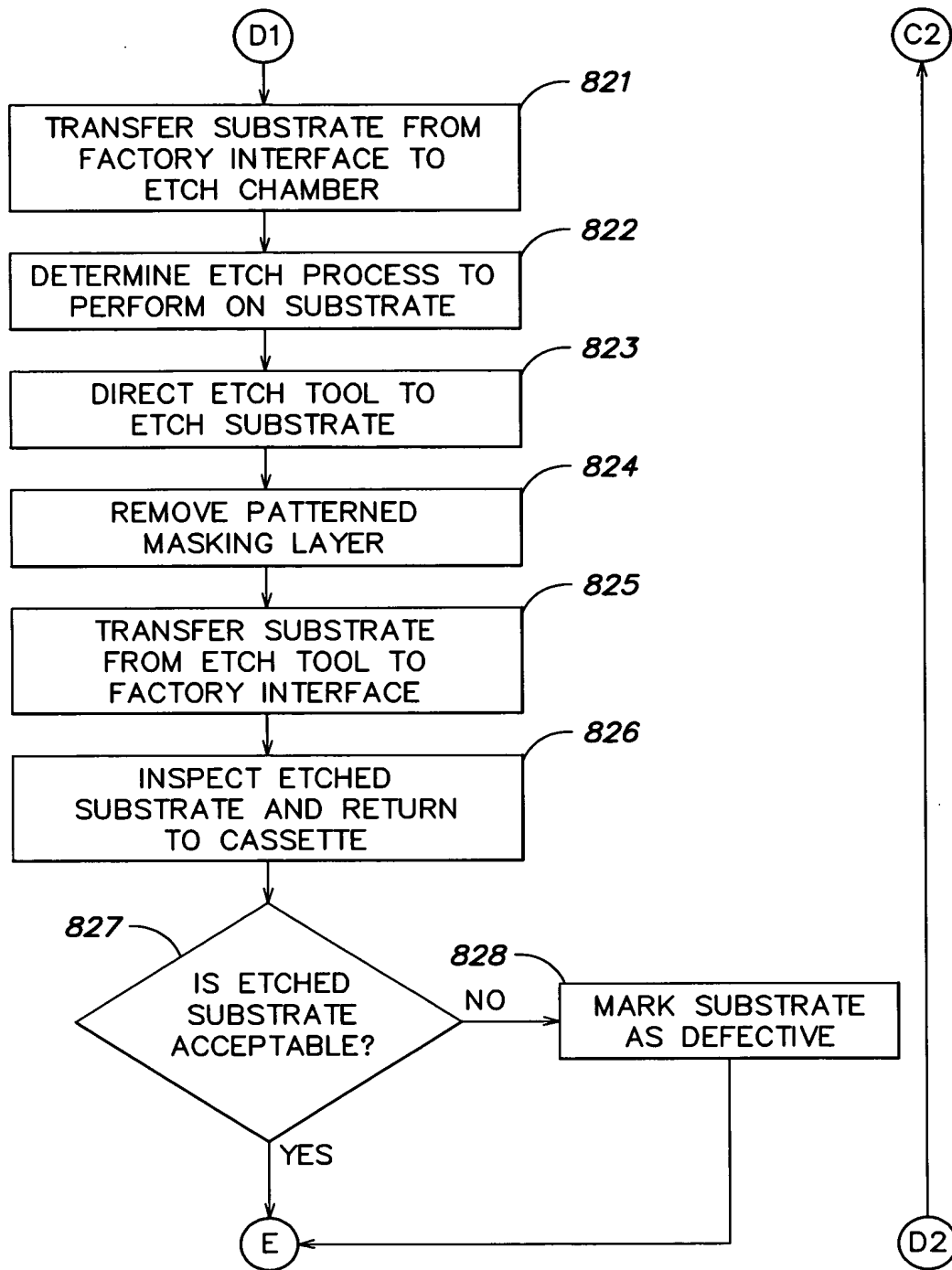


FIG. 8D

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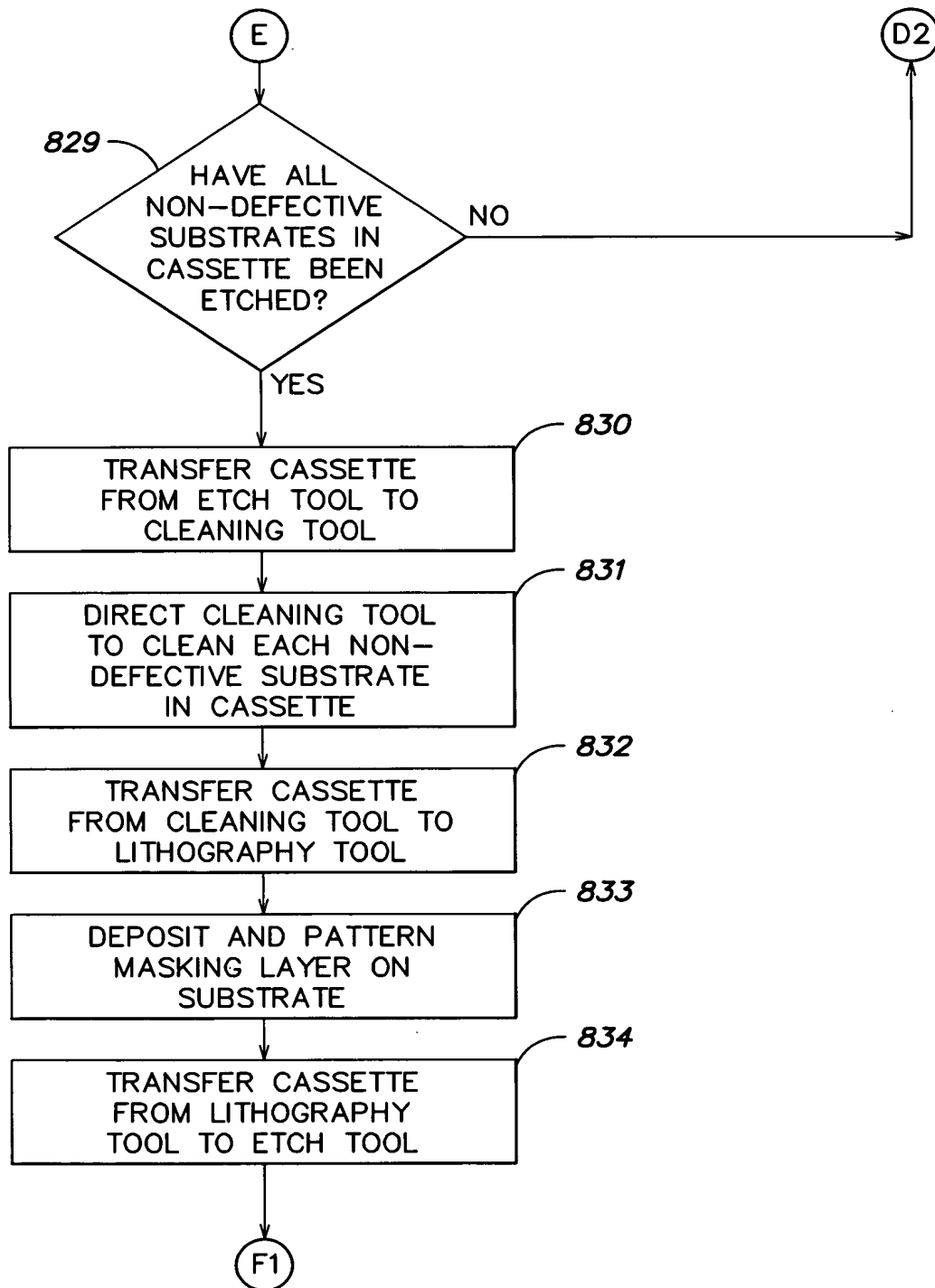


FIG. 8E

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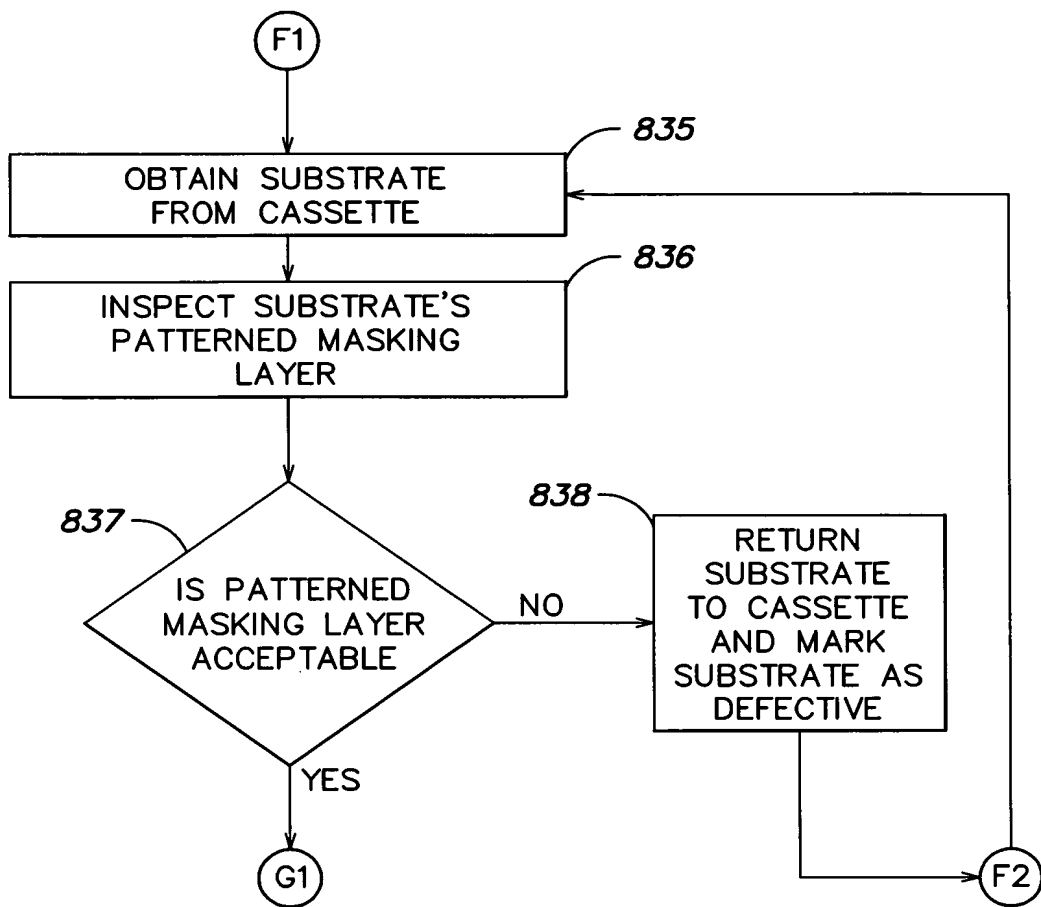


FIG. 8F

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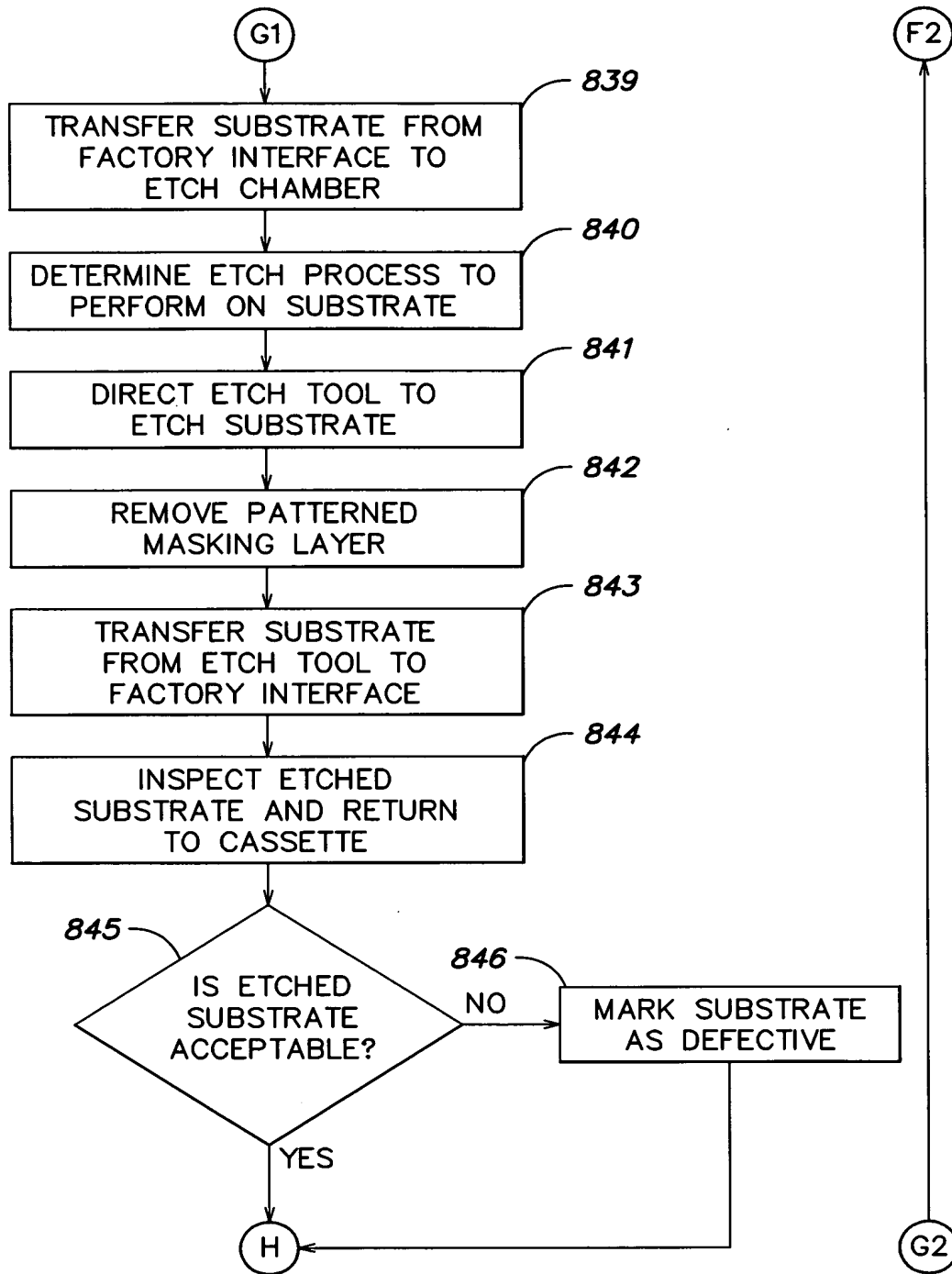


FIG. 8G

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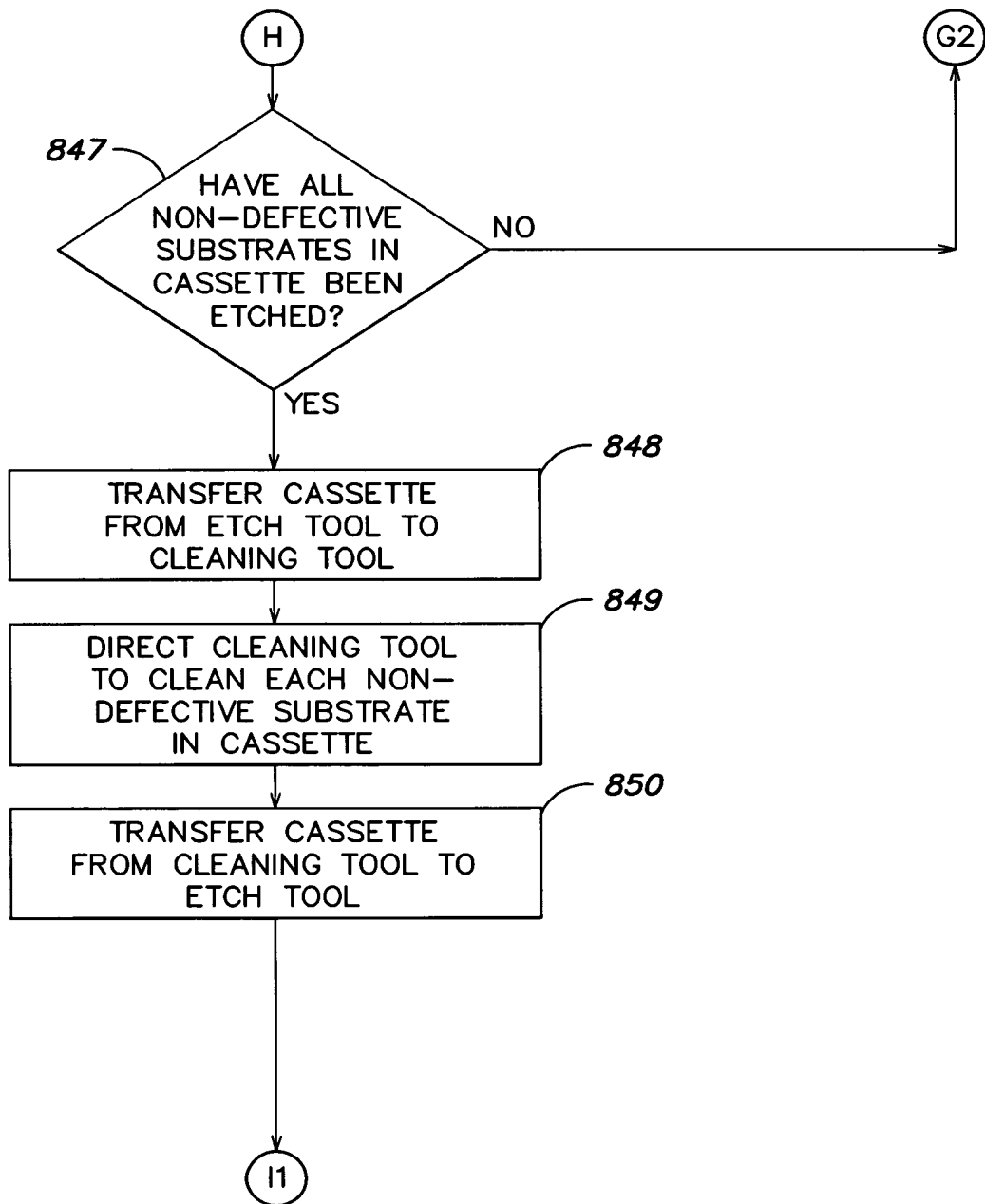


FIG. 8H

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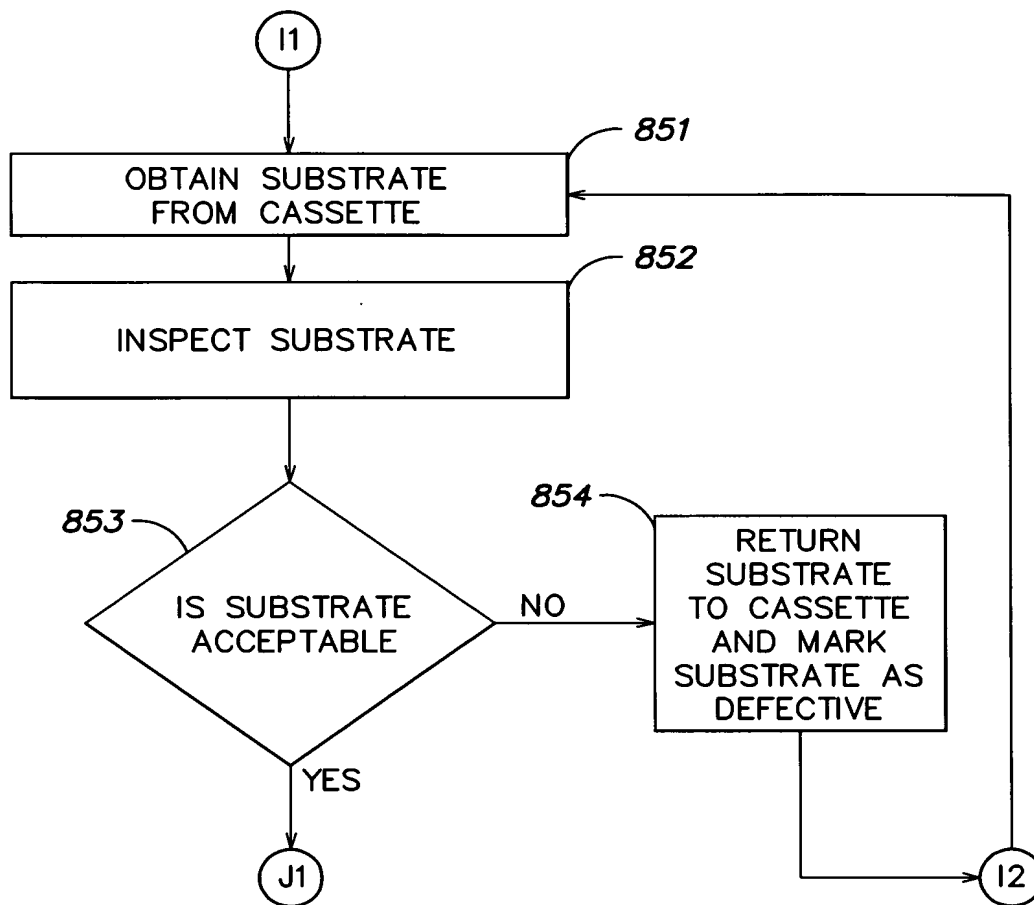


FIG. 81

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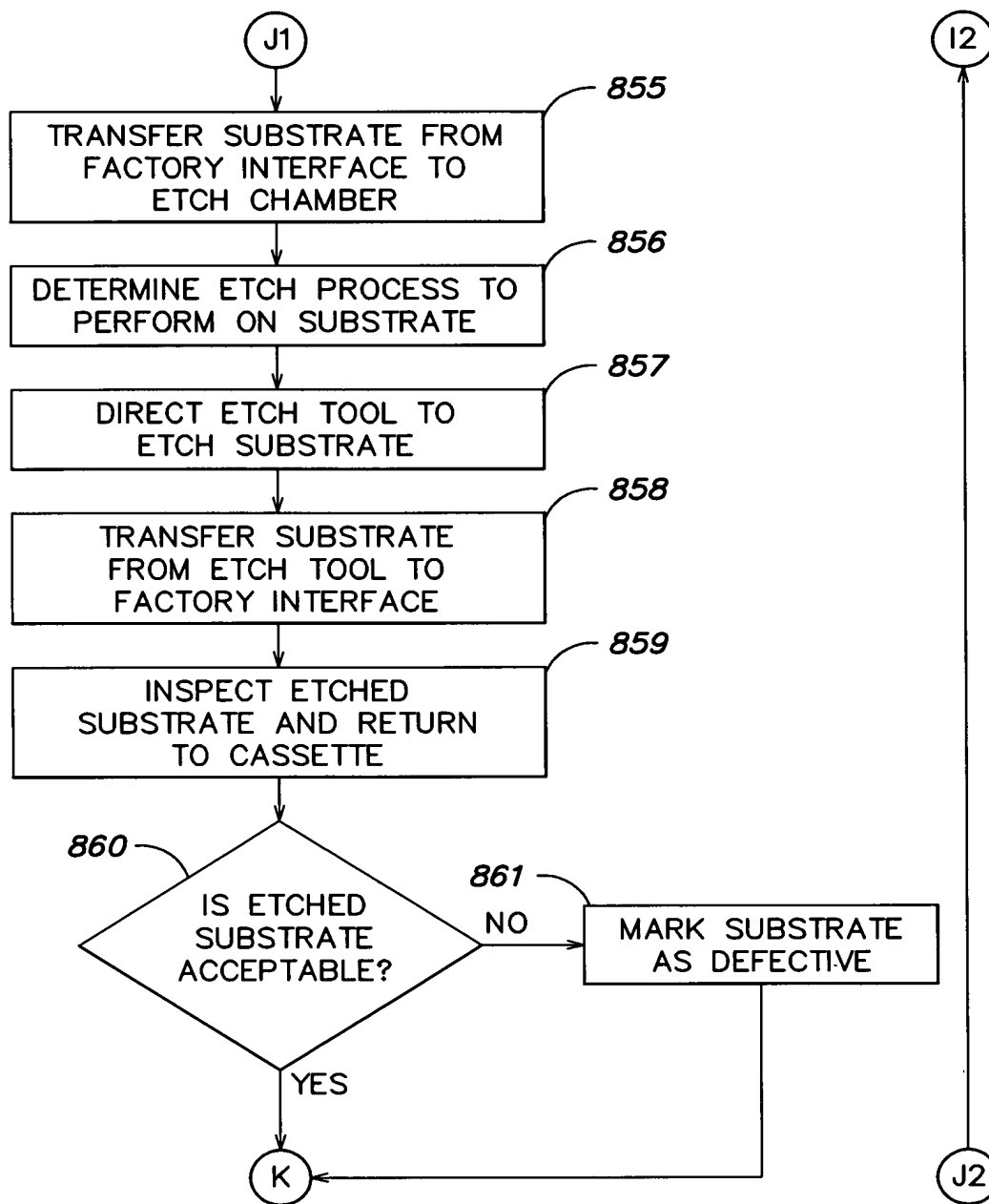


FIG. 8J

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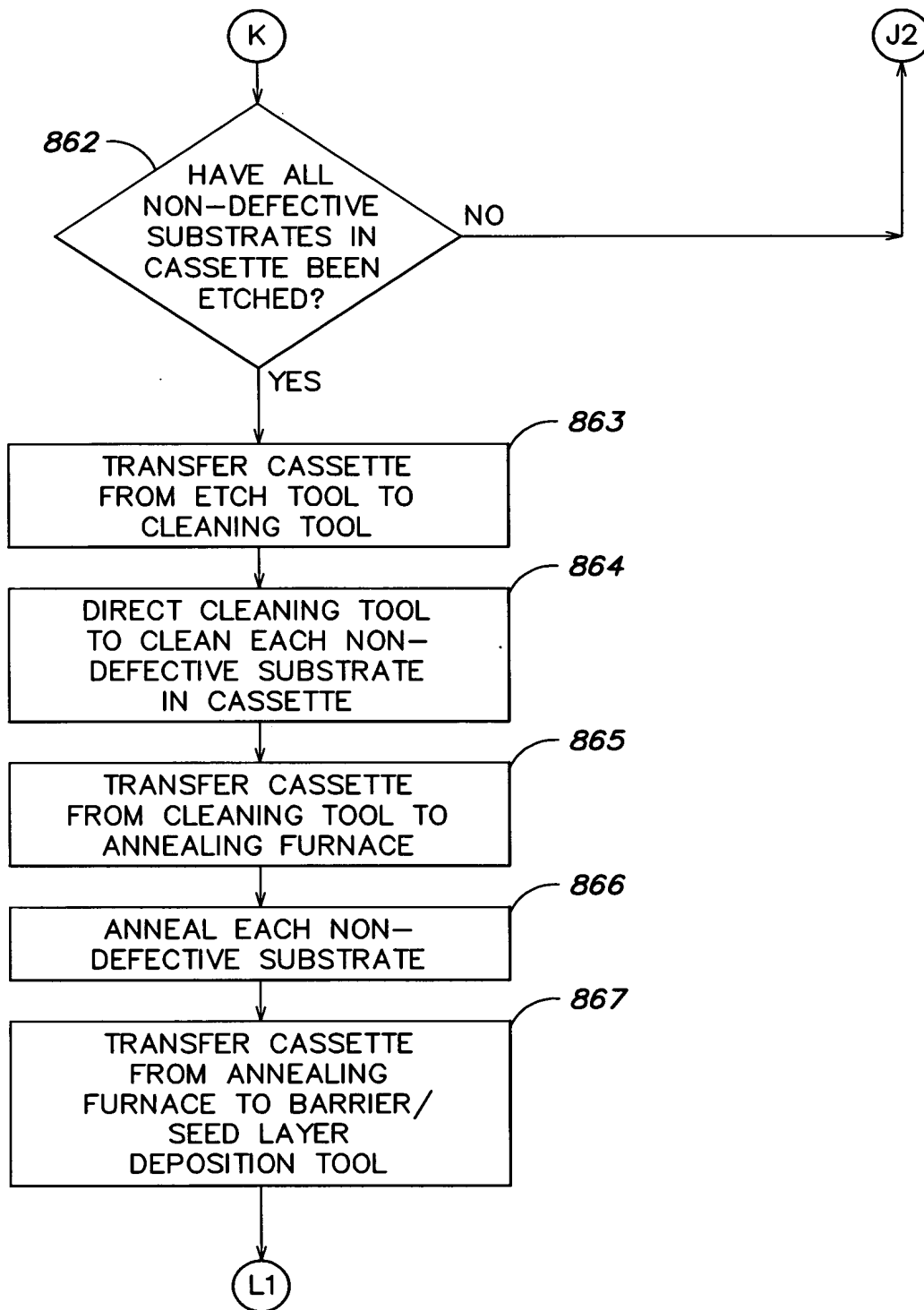


FIG. 8K

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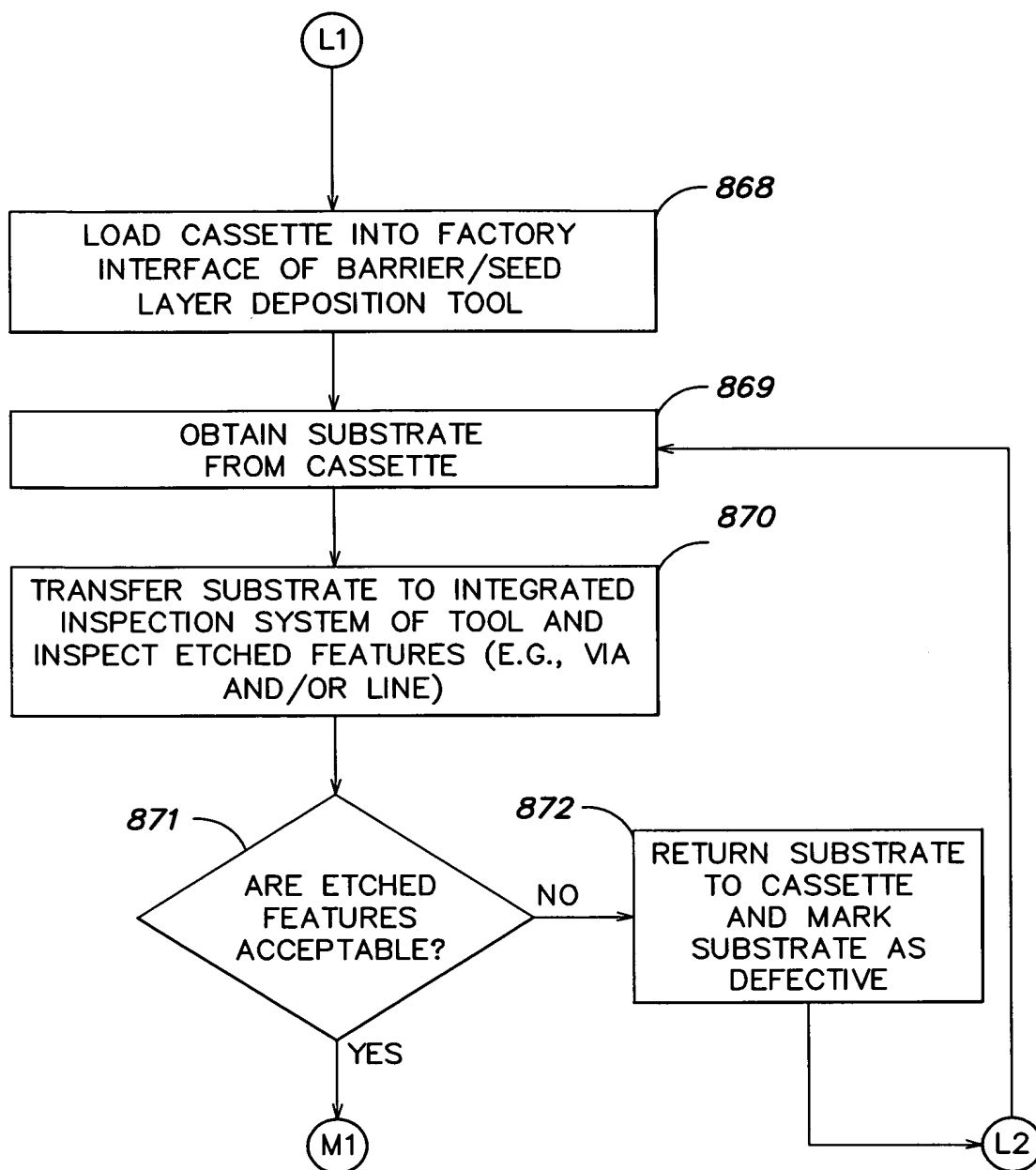


FIG. 8L

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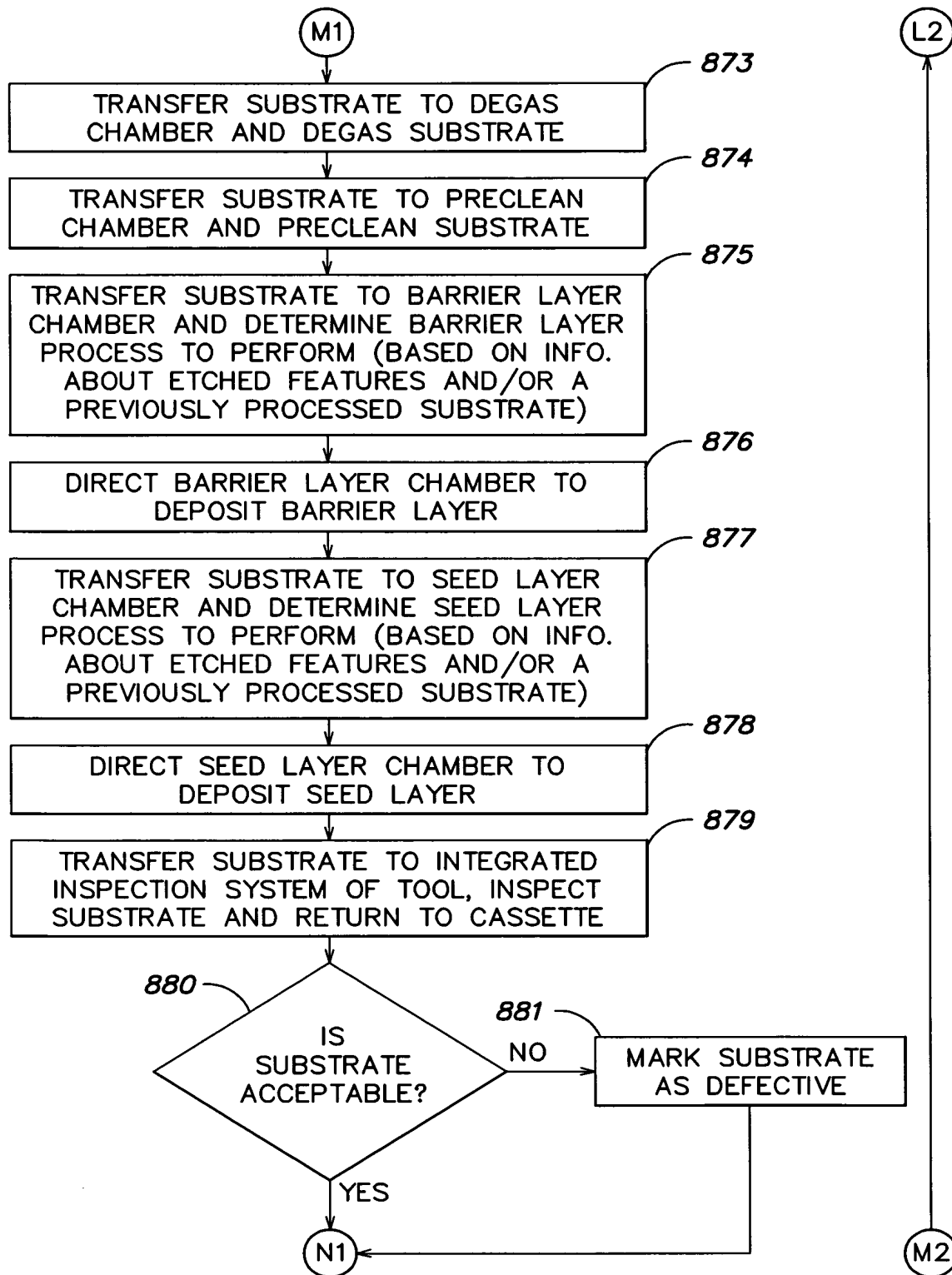
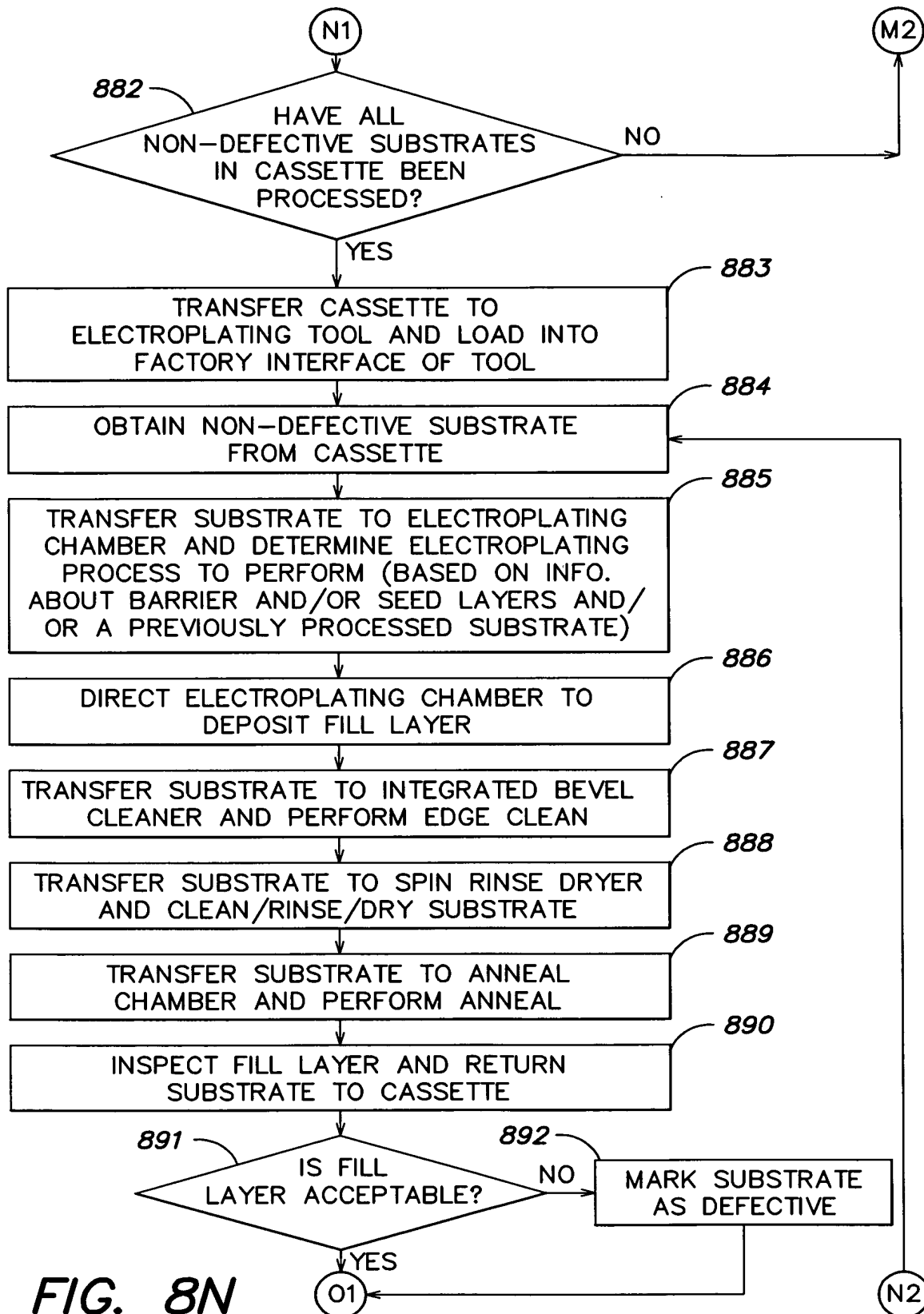


FIG. 8M

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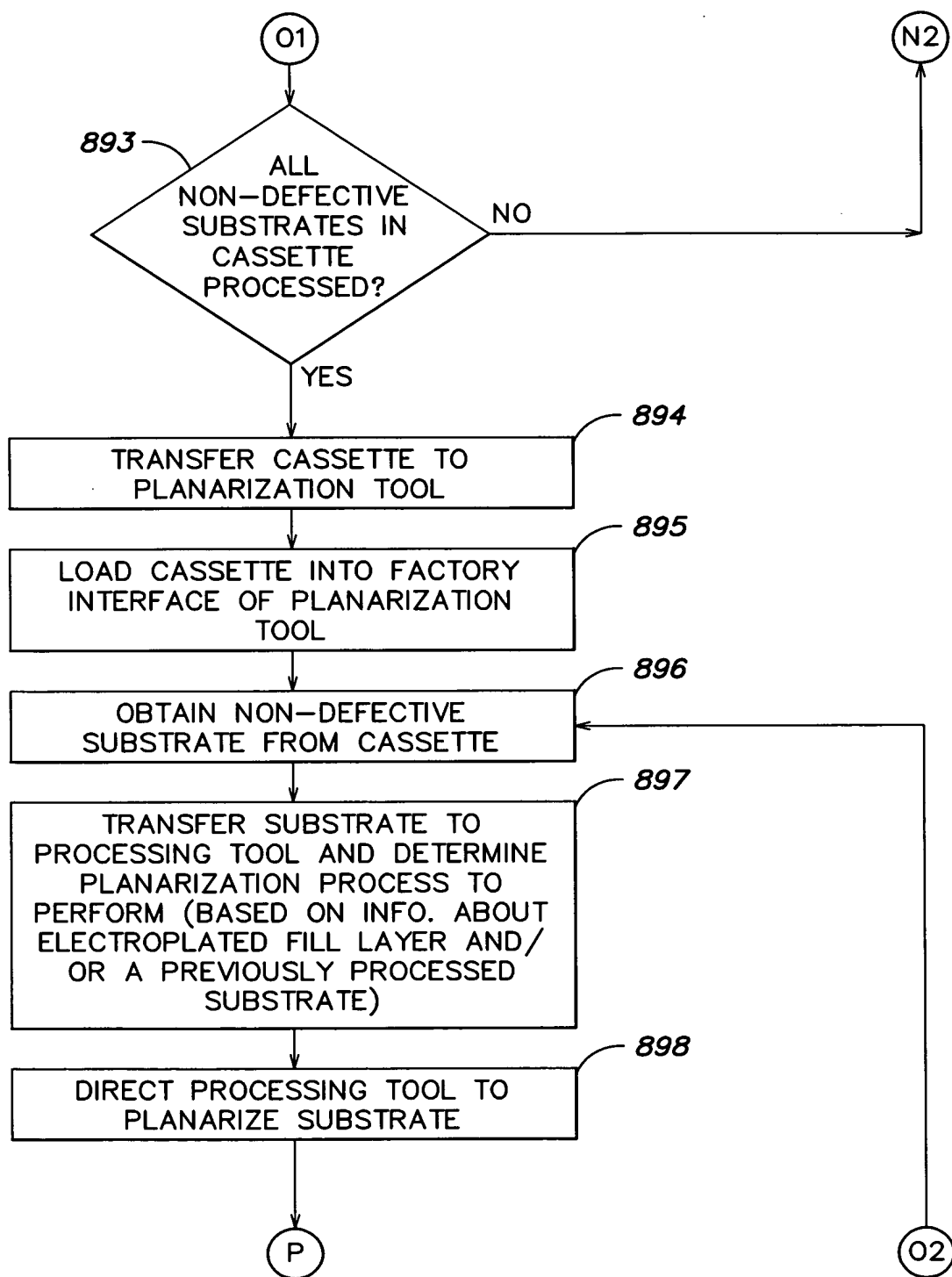


FIG. 80

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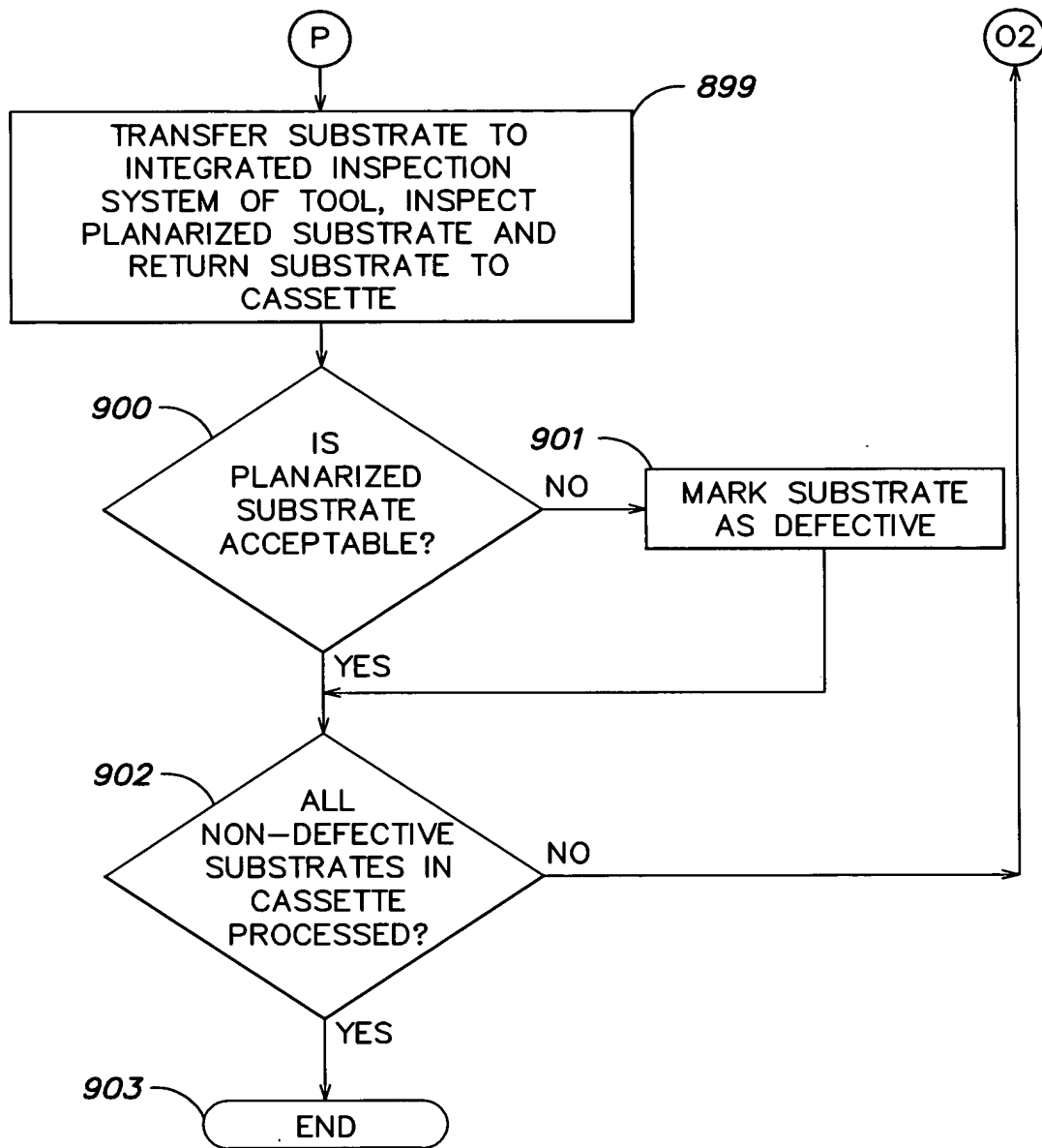


FIG. 8P

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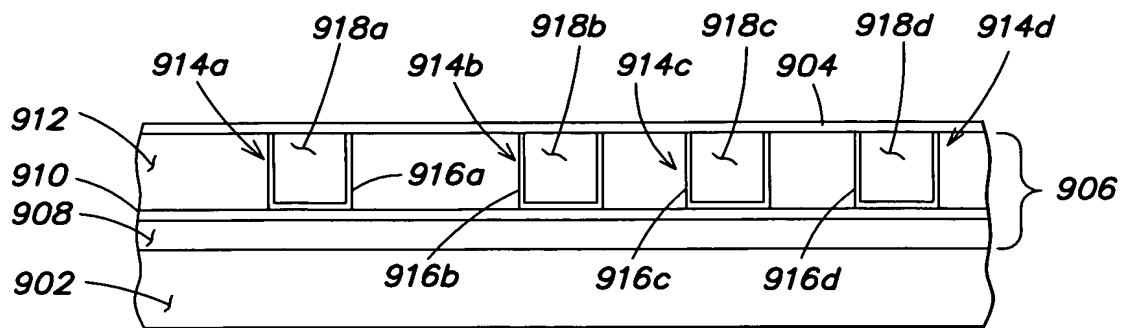


FIG. 9A

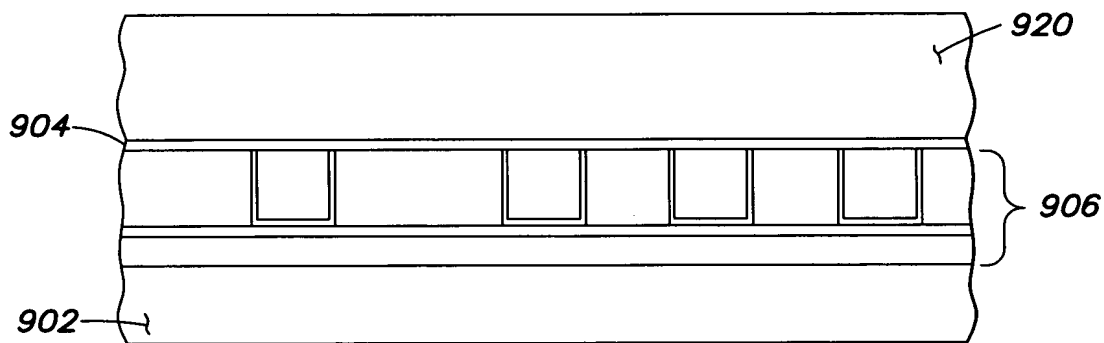


FIG. 9B

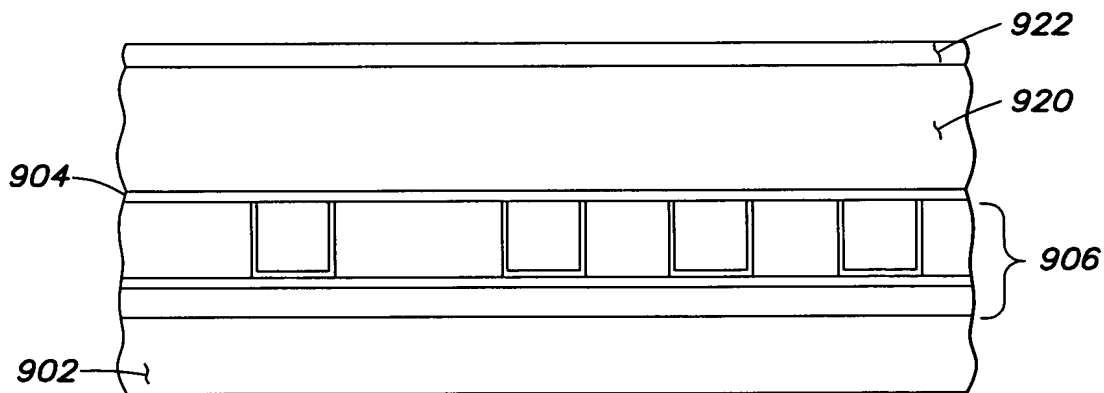


FIG. 9C

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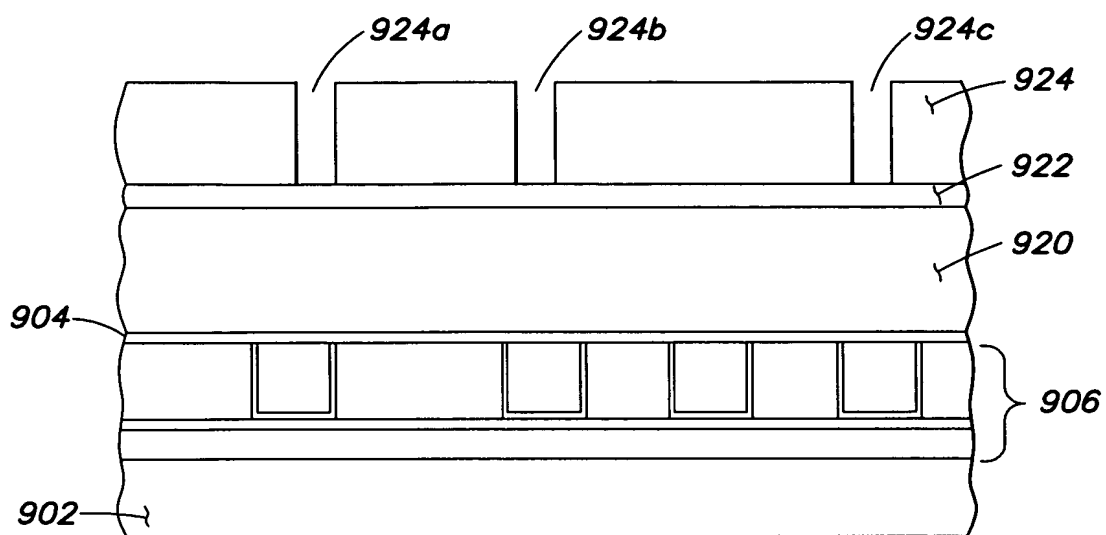


FIG. 9D

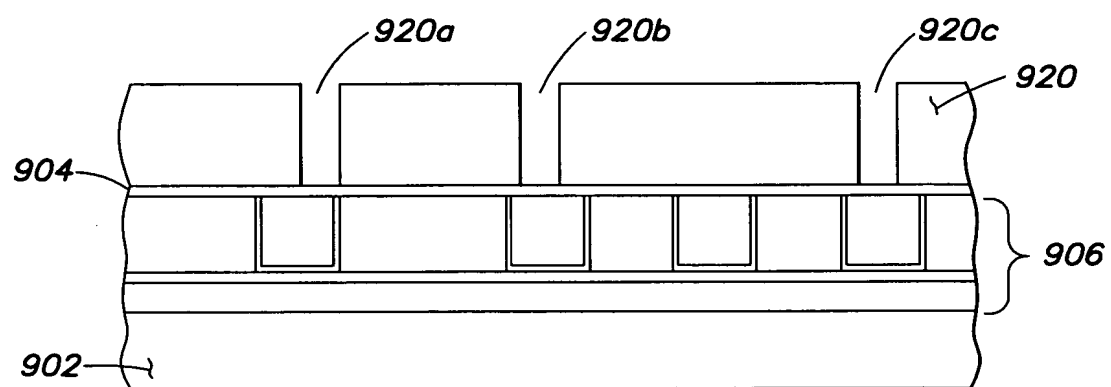


FIG. 9E

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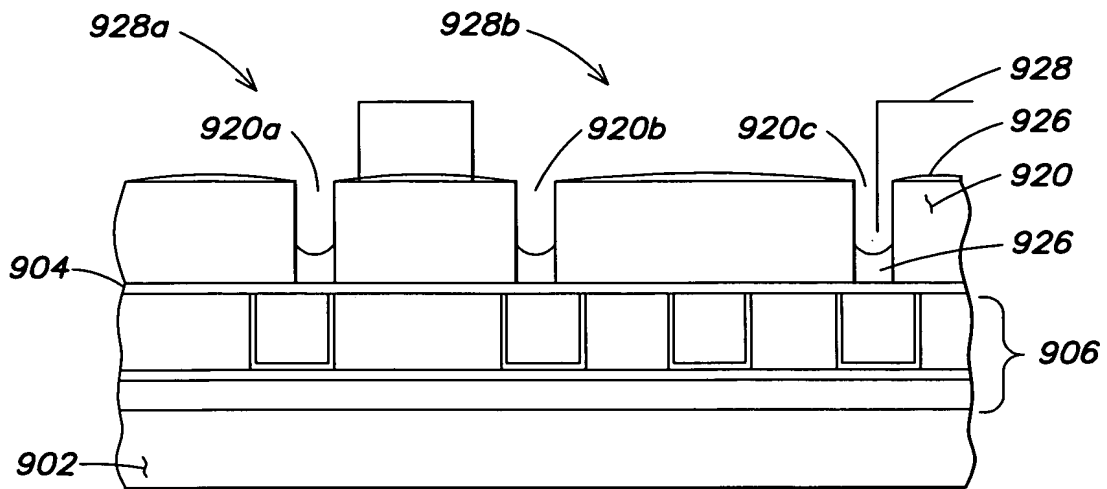


FIG. 9F

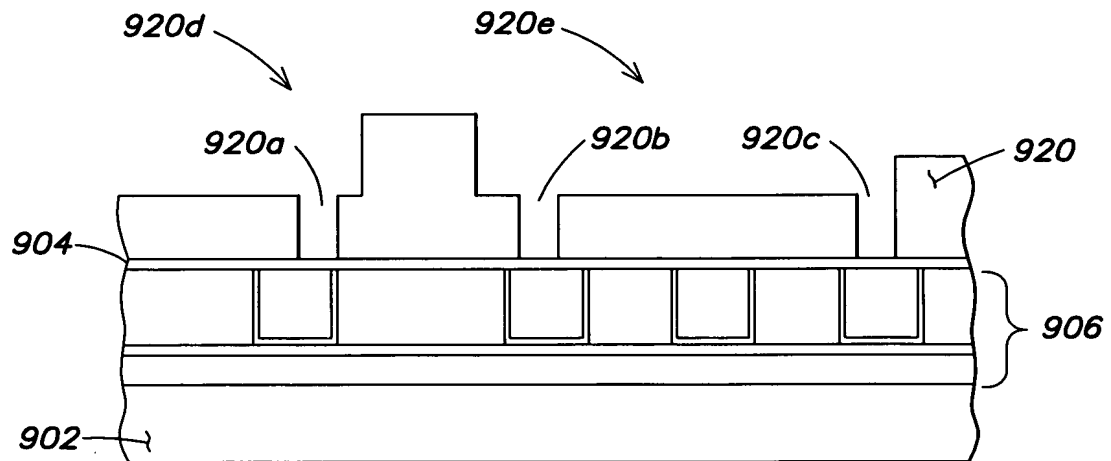


FIG. 9G

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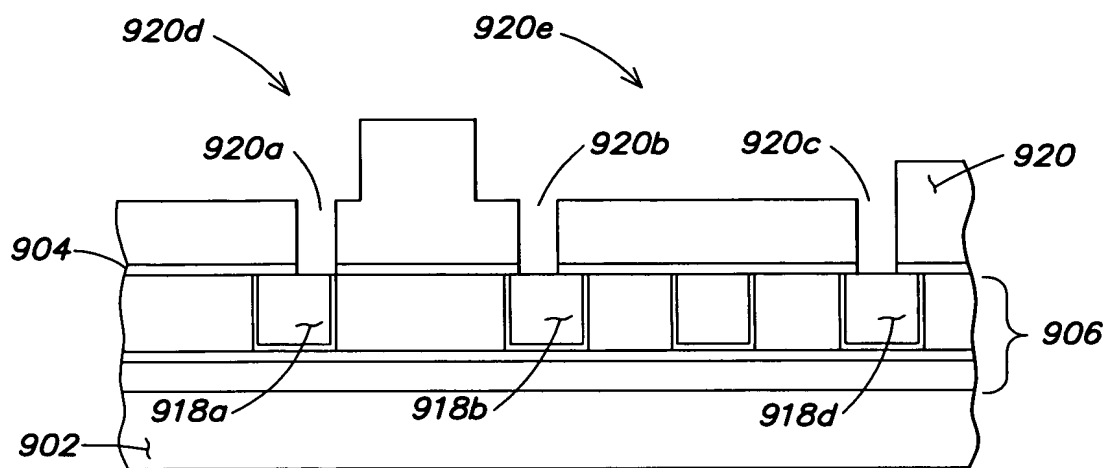


FIG. 9H

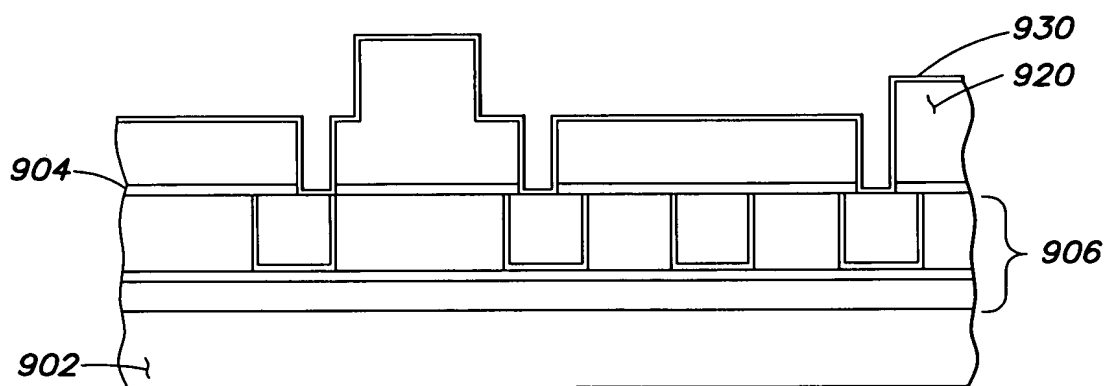


FIG. 9I

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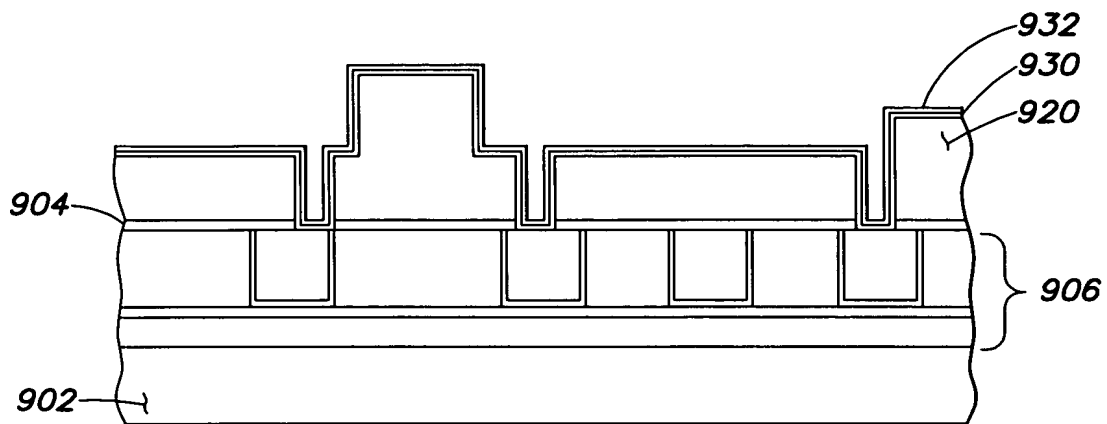


FIG. 9J

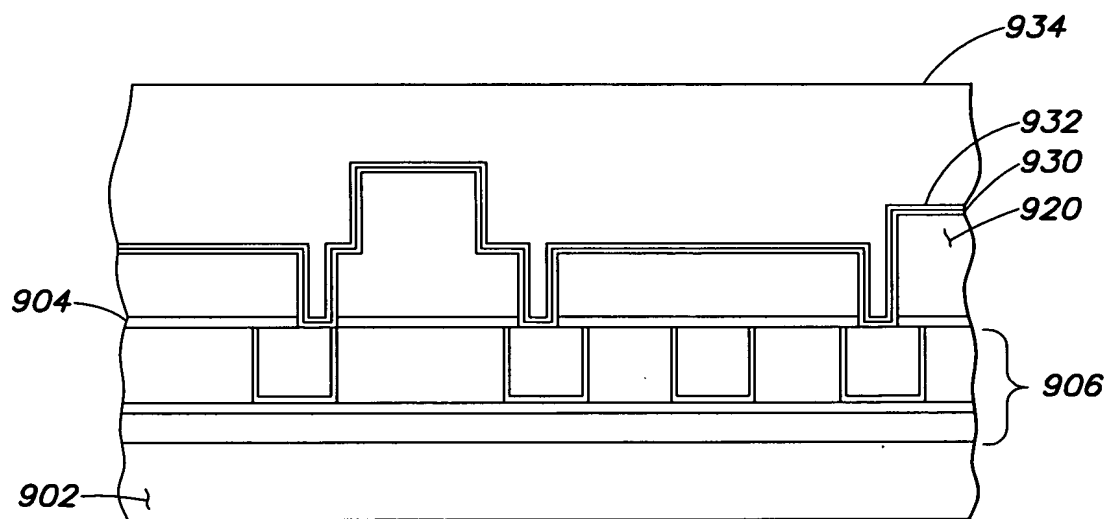


FIG. 9K

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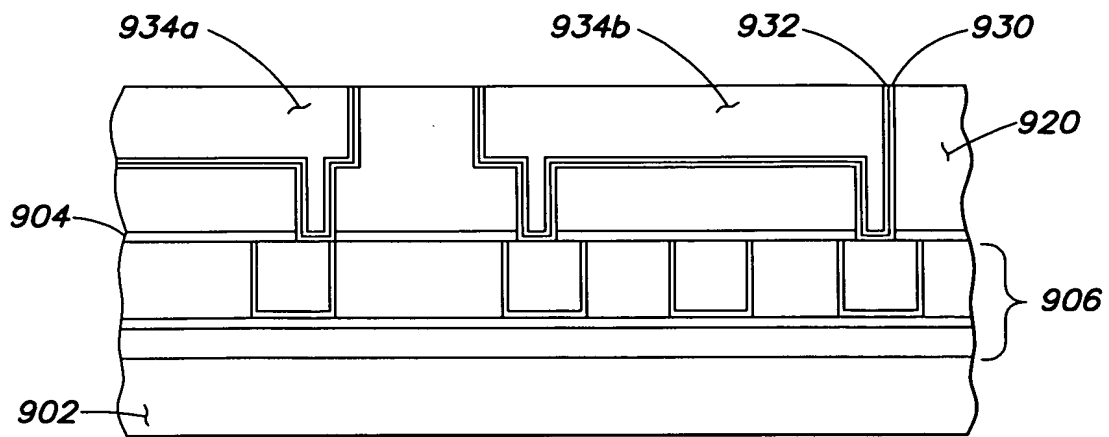


FIG. 9L

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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Deposition within low K dielectric deposition tool 102	Feedforward information about interconnect features to be formed (e.g., density, dimensions, profile, etc.)	Chamber base pressure, processing pressure, processing temperature, processing time, processing power, gas flow rates, gas flow ratios, deposition time	Alters thickness, dielectric constant, stress level, refractive index, defect density and/or uniformity of deposited low K dielectric
Deposition within low K dielectric deposition tool 102	Feedback information about previously deposited low K dielectric (e.g., thickness, dielectric constant, stress level, index of refraction, uniformity, etc.)	Chamber base pressure, processing pressure, processing temperature, processing time, processing power, gas flow rates, gas flow ratios, deposition time	Alters thickness, dielectric constant, stress level, refractive index, defect density and/or uniformity of deposited low K dielectric
Clean within low K dielectric deposition tool 102	Feedback information about measured defect density following deposition	1. Clean time or frequency of cleaning;	1. Alters clean time or frequency of cleaning (to maintain desired defect density – e.g., increase one or both to reduce defect density);
		2. Season time;	2. Alters season time (to maintain desired defect density – increase to reduce defect density);

FIG. 10A

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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Etching within etch tool 106	Feedforward information about patterned masking layer (e.g., pattern density, feature dimensions, feature profile, etc.)	1. Select previously optimized process recipe based on pattern density;	1. Adjusts process based on selected process recipe, actual pattern density and desired etch results;
		Chamber base pressure, processing pressure, etch time, source power, substrate bias power, gas flow rates, gas flow ratios, deposition time, magnetic field strength	Adjusts etched feature depth, width and/or profile, uniformity, etc.
Etching within etch tool 106	Feedback information about previously etched features (e.g., dimensions or profile)	Chamber base pressure, processing pressure, etch time, source power, substrate bias power, gas flow rates, gas flow ratios, deposition time, magnetic field strength	Adjusts etched feature depth, width and/or profile, uniformity, etc.

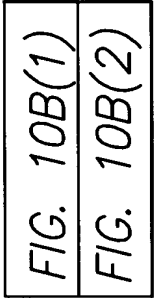
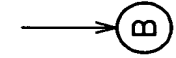


FIG. 10B(1)

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
INTERCONNECT ON A SUBSTRATE
Inventor(s): Hongwen Li, Lee Luo, Ilias Iliopoulos and
Michael D. Armacost
Serial No.: 10/759,801
Filing Date: January 16, 2004

Express Mail Label No.: EV605116109US

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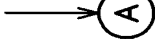
<div data-bbox="261 1732 415 1787">  </div>		Clean within etch tool 106	
		Feedback information about previously measured defect density following etching	
	1. Chamber clean time or frequency of cleaning or season time;		1. Alters clean time or frequency of cleaning or season time (to maintain desired defect density – e.g., increase one or more to reduce defect density);
	2. O ₂ flow;		2. Alters O ₂ flow rate (e.g., increase O ₂ flow to increase polymeric residue removal)
	3. Source power;		3. Alters source power (e.g., increase source power to remove residue faster);

FIG. 10B(2)

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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Barrier Layer Deposition Within Tool 112	Feedforward Information About Etched Features (e.g., Via and/or Line Dimensions)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Barrier Layer Deposition Within Tool 112	Feedback Information About Previously Deposited Barrier Layer (e.g., Layer Thickness)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Barrier Layer Deposition Within Tool 112	Feedback Information About Previously Measured Defect Density Following Barrier Layer Deposition	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Seed Layer Deposition Within Tool 112	Feedforward Information About Etched Features (e.g., Via and/or Line Dimensions)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Seed Layer Deposition Within Tool 112	Feedback Information About Previously Deposited Seed Layer (e.g., Layer Thickness)	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.
Seed Layer Deposition Within Tool 112	Feedback Information About Previously Measured Defect Density Following Seed Layer Deposition	RF Bias, DC Power, Base Pressure, Process Time or Pressure, Temperature, Wafer Bias, KWH.	Alters Rs, Reflectivity, Thickness, Defects, Uniformity. For Blanket as Well as Patterned Areas.

FIG. 10C

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
INTERCONNECT ON A SUBSTRATE
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Serial No.: 10/759,801
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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Electroplating Within Tool 114	Feedforward Information About Barrier Layer (From Tool 112)	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.
Electroplating Within Tool 114	Feedforward Information About Seed Layer (From Tool 112)	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.
Electroplating Within Tool 114	Feedback Information About Previously Electroplated Fill Layer (e.g., Layer Thickness)	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.
Electroplating Within Tool 114	Feedback Information About Previously Measured Defect Density Following Electroplating	A), B) and/or C) Below	Alters Thickness, Rs, Uniformity, Reflectivity, Gap Fill, Defects, Backside Contamination. For Blanket as Well as Patterned Areas.

- A) ECP Plating Process: Flow Rate; Z-Height; Rotation Rate; Plating Recipe (e.g., Current and/or Voltage); Immersion Rotation Rate; Anode Amp-Hr; and/or Contact Ring Amp-Hr
- B) Electrolyte/Bath Process: Temperature; Chemistry; Chemical Acidity; and/or Flow Rate
- C) Anneal Process: Temperature Uniformity; Gas Flow Rates; and/or Pressure Before, During or After Anneal

FIG. 10D

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
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PROCESS ADJUSTED	BASIS FOR ADJUSTMENT	PROCESS PARAMETERS ADJUSTED	AFFECT OF ADJUSTMENT
Planarization within tool 116	Feedforward information about electroplated fill layer (from tool 114)	Retaining ring pressure; Membrane or inner tube pressure; slurry or rinsing fluid flow rate; head pressure or velocity; slurry rate/type/concentration; polish/rinse/dry/cleaning time; substrate rotation rate.	Alters thickness, profile, Rs, uniformity. For blanket as well as patterned areas.
Planarization within tool 116	Feedback information about previously planarized surface (e.g., surface planarity)	Retaining ring pressure; Membrane or inner tube pressure; slurry or rinsing fluid flow rate; head pressure or velocity; slurry rate/type/concentration; polish/rinse/dry/cleaning time; substrate rotation rate.	Alters thickness, profile, Rs, uniformity. For blanket as well as patterned areas.
Planarization within tool 116	Feedback information about previously measured defect density following planarization	Retaining ring pressure; Membrane or inner tube pressure; slurry or rinsing fluid flow rate; head pressure or velocity; slurry rate/type/concentration; polish/rinse/dry/cleaning time; substrate rotation rate.	Alters thickness, profile, Rs, uniformity. For blanket as well as patterned areas.

FIG. 10E

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
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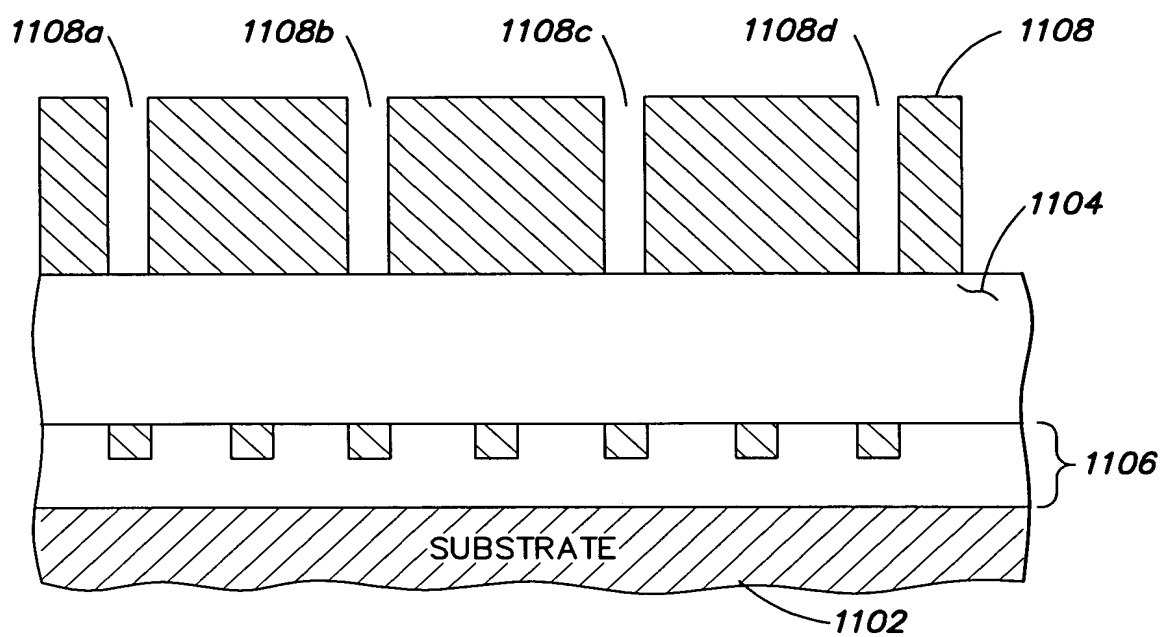


FIG. 11

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
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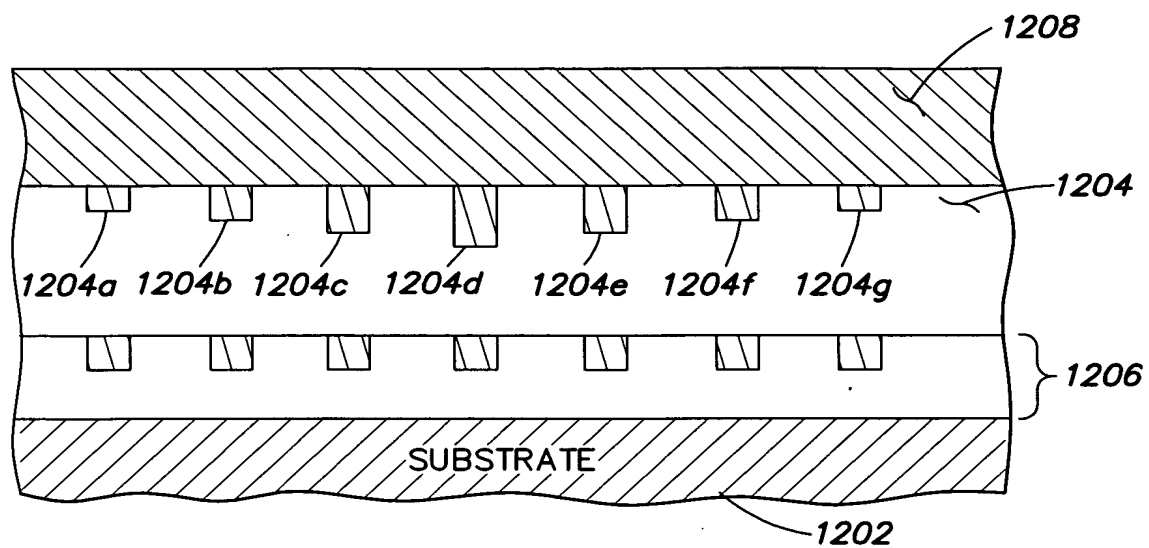


FIG. 12A

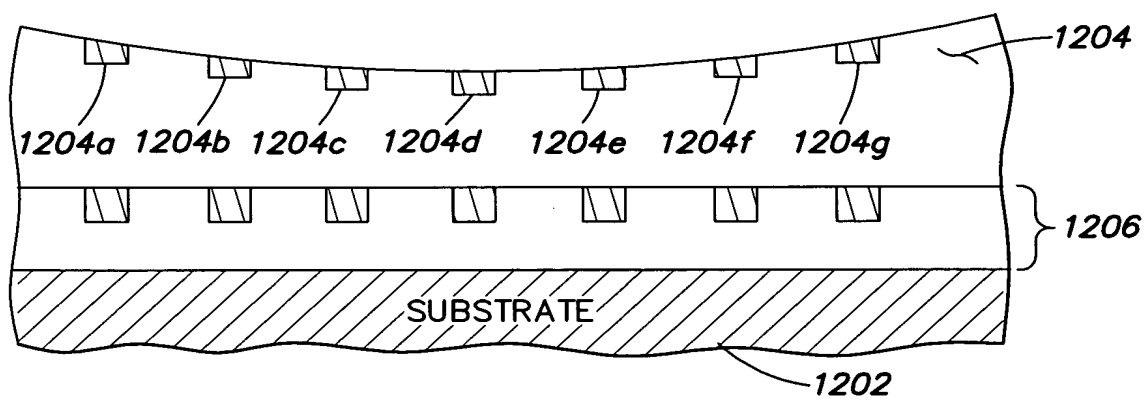


FIG. 12B

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
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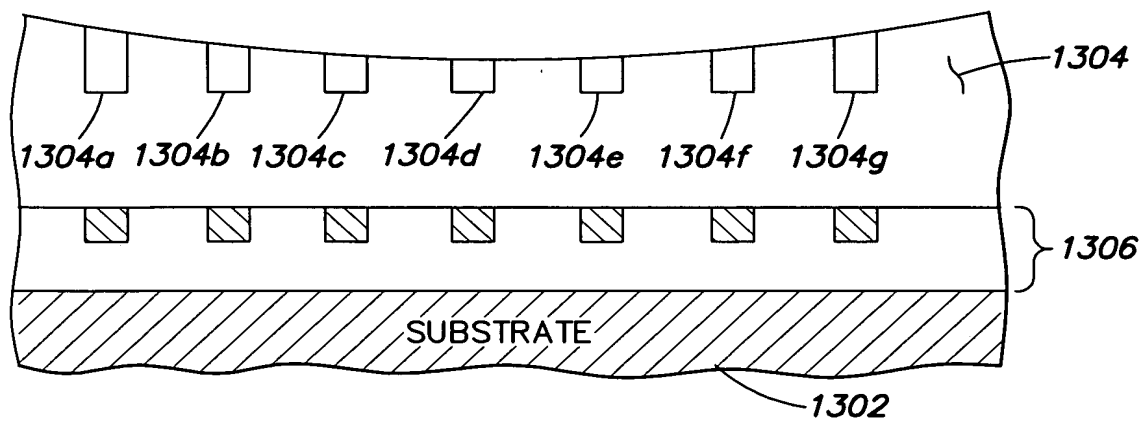


FIG. 13A

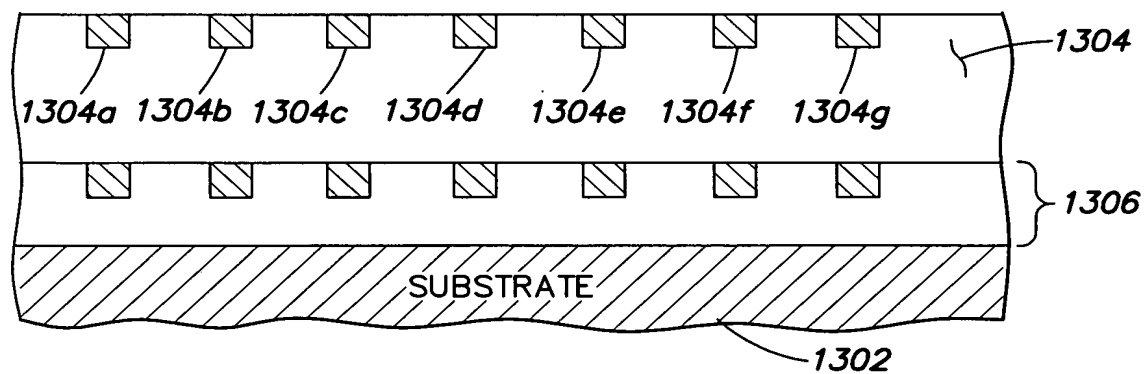


FIG. 13b

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
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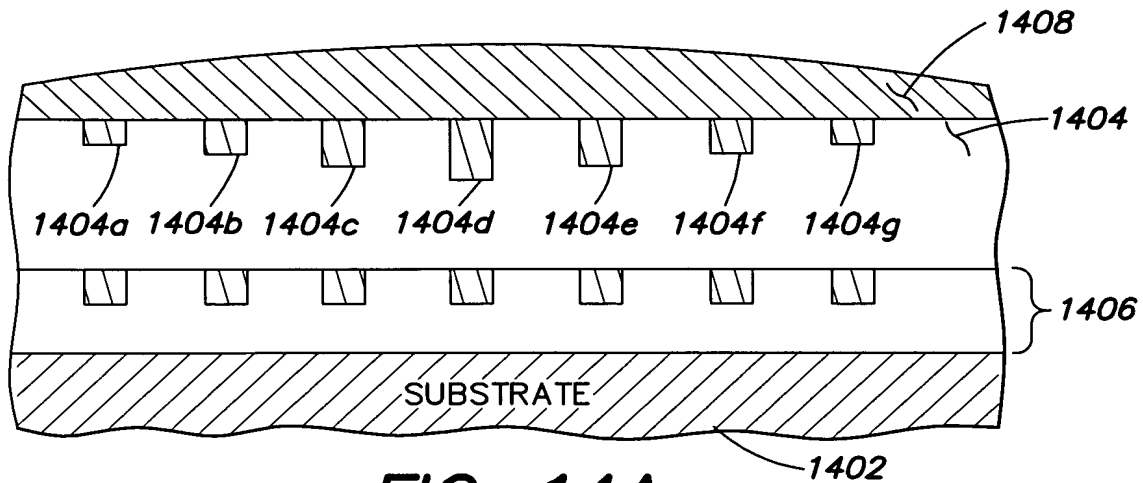


FIG. 14A

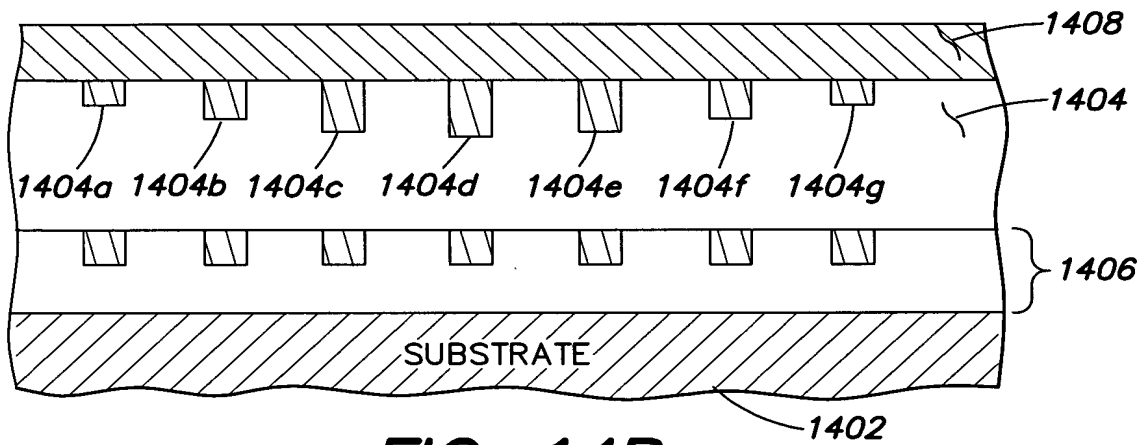


FIG. 14B

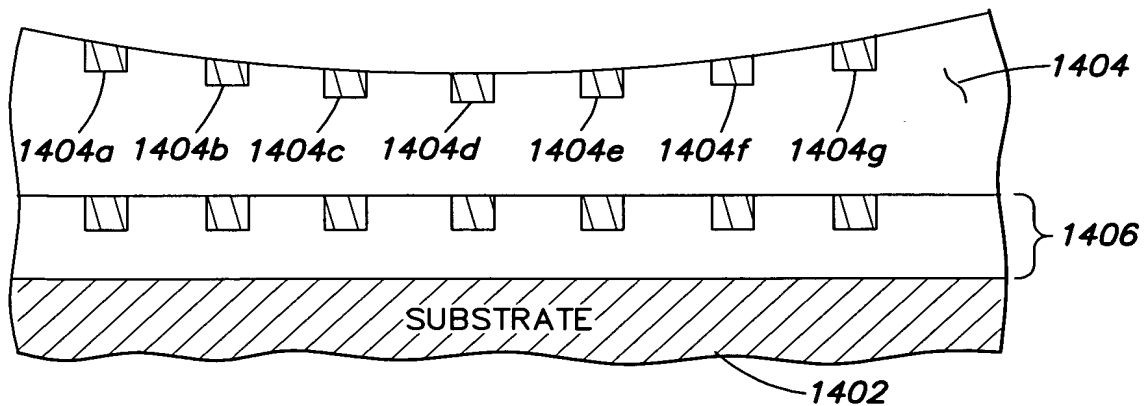


FIG. 14C

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
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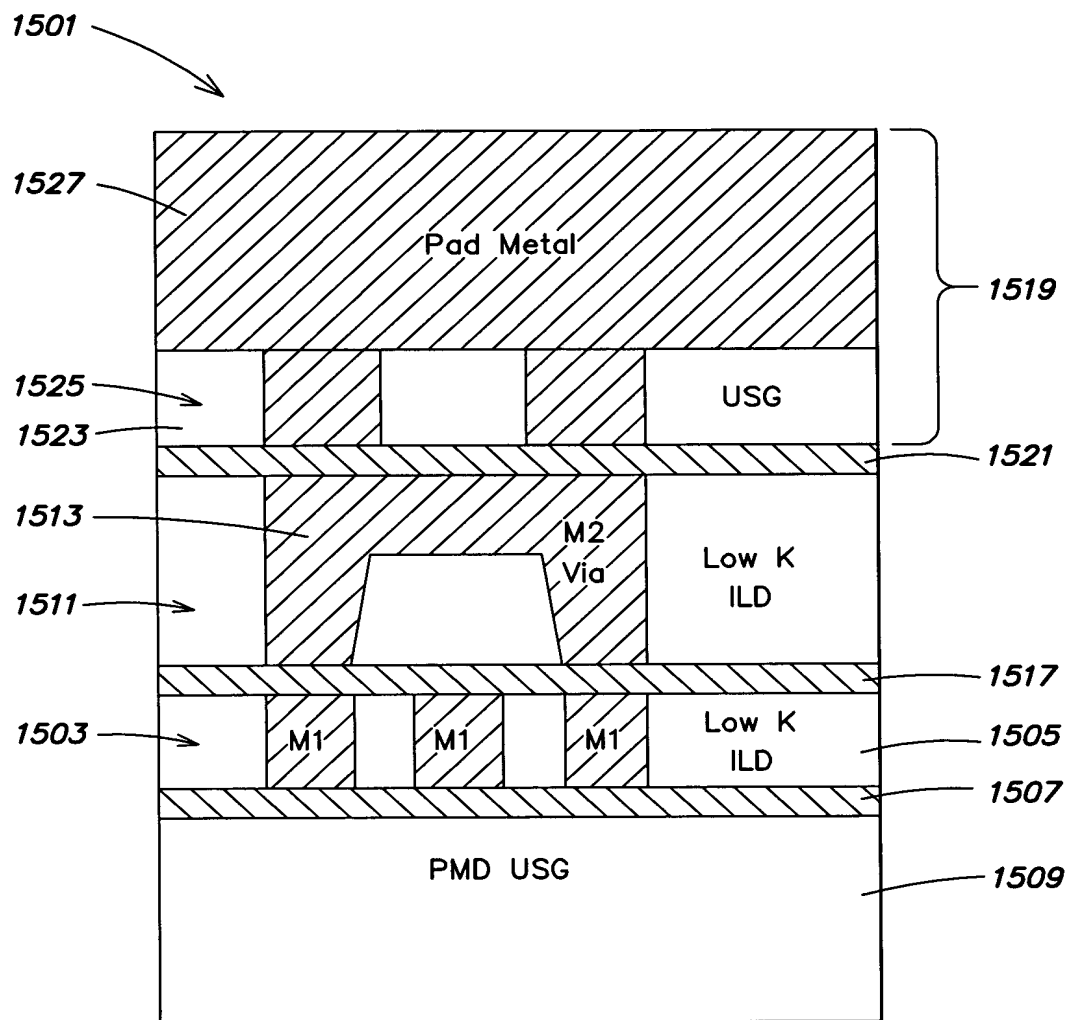


FIG. 15

Re: Applied Materials Docket No.: 6353/P1/LOW K/JW
INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC
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